

It turns out we can say a bit more about the timing of output transitions for CMOS logic gates.

Let's start by considering the behavior of a non-CMOS combinational device that implements the NOR function.

Looking at the waveform diagram, we see that initially the A and B inputs are both 0, and the output Z is 1, just as specified by the truth table.

Now B makes a 0-to-1 transition and the Z output will eventually reflect that change by making a 1-to-0 transition.

As we learned in the previous video, the timing of the Z transition is determined by the contamination and propagation delays of the NOR gate.

Note that we can't say anything about the value of the Z output in the interval of  $t_{CD}$  to  $t_{PD}$  after the input transition, which we indicate with a red shaded region on the waveform diagram.

Now, let's consider a different set up, where initially both A and B are 1, and, appropriately, the output Z is 0.

Examining the truth table we see that if A is 1, the output Z will be 0 regardless of the value of B.

So what happens when B makes a 1-to-0 transition?

Before the transition, Z was 0 and we expect it to be 0 again,  $t_{PD}$  after the B transition.

But, in general, we can't assume anything about the value of Z in the interval between  $t_{CD}$  and  $t_{PD}$ .

Z could have any behavior it wants in that interval and the device would still be a legitimate combinational device.

Many gate technologies, e.g., CMOS, adhere to even tighter restrictions.

Let's look in detail at the switch configuration in a CMOS implementation of a NOR gate when both inputs are a digital 1.

A high gate voltage will turn on NFET switches (as indicated by the red arrows) and turn off PFET switches (as indicated by the red "Xs").

Since the pullup circuit is not conducting and the pulldown circuit is conducting, the output Z is connected to GROUND, the voltage for a digital 0 output.

Now, what happens when the B input transitions from 1 to 0?

The switches controlled by B change their configuration: the PFET switch is now on and the NFET switch is now

off.

But overall the pullup circuit is still not conducting and there is still a pulldown path from Z to GROUND.

So while there used to be two paths from Z to GROUND and there is now only one path, Z has been connected to GROUND the whole time and its value has remained valid and stable throughout B's transition.

In the case of a CMOS NOR gate, when one input is a digital 1, the output will be unaffected by transitions on the other input.

A lenient combinational device is one that exhibits this behavior, namely that the output is guaranteed to be valid when any combination of inputs sufficient to determine the output value has been valid for at least  $t_{PD}$ .

When some of the inputs are in a configuration that triggers this lenient behavior, transitions on the other inputs will have no effect on the validity of the output value.

Happily most CMOS implementations of logic gates are naturally lenient.

We can extend our truth-table notation to indicate lenient behavior by using "X" for the input values on certain rows to indicate that input value is irrelevant when determining the correct output value.

The truth table for a lenient NOR gate calls out two such situations: when A is 1, the value of B is irrelevant, and when B is 1, the value of A is irrelevant.

Transitions on the irrelevant inputs don't trigger the  $t_{CD}$  and  $t_{PD}$  output timing normally associated with an input transition.

When does lenience matter?

We'll need lenient components when building memory components, a topic we'll get to in a couple of chapters.

You're ready to try building some CMOS gates of your own!

Take a look at the first lab exercise in Assignment 2.

I think you'll find it fun to work on!