Computation Structures

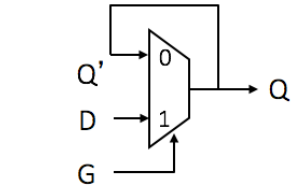
Sequential Logic Worksheet

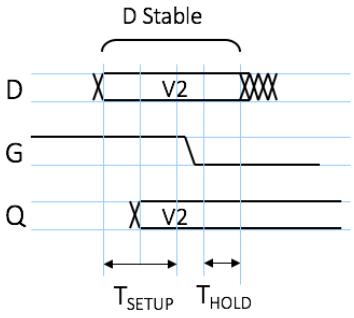
Concept Inventory:

- D-latch & the Dynamic Discipline
- D-register
- Timing constraints for sequential circuits
- Set-up and hold times for sequential circuits

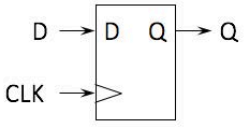
Notes:

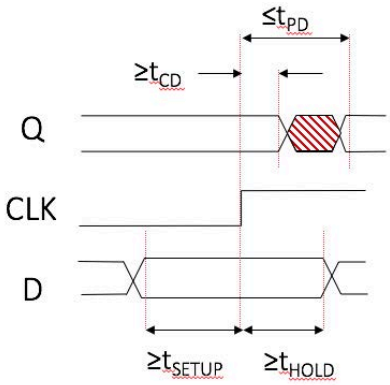
D latch

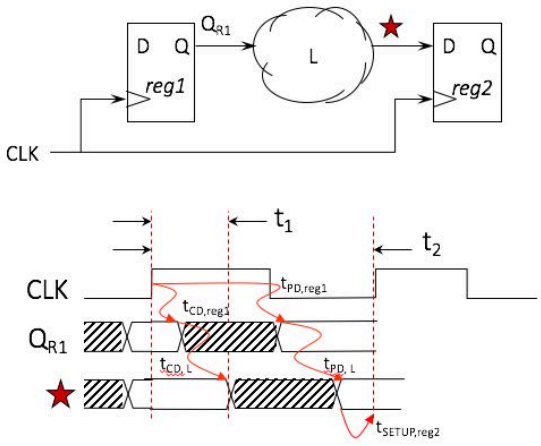




D register

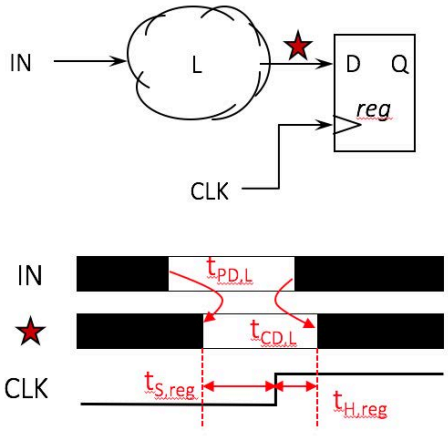






$t_1 = t_{CD,reg1} + t_{CD,L} \geq t_{HOLD,reg2}$

$t_2 = t_{PD,reg1} + t_{PD,L} + t_{SETUP,reg2} \leq t_{CLK}$

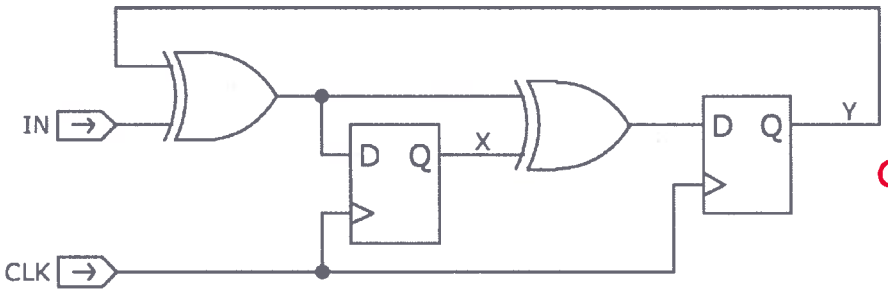


$t_{S,INPUT} = t_{PD,L} + t_{S,R}$

$t_{H,INPUT} = t_{H,R} - t_{CD,L}$

Problem 1.

Consider the following sequential logic circuit. It consists of one input IN, a 2-bit register that stores the current state, and some combinational logic that determines the state (next value to load into the register) based on the current state and the input IN.



GOAL: Dynamic discipline obeyed at input to each register

(A) Using the timing specifications shown below for the XOR and DREG components, determine the shortest clock period, t_{CLK}, that will allow the circuit to operate correctly or write NONE if no choice for t_{CLK} will allow the circuit to operate correctly and briefly explain why.

Component	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
XOR2	0.15ns	2.1ns	–	–
DREG	0.1ns	1.6ns	0.4ns	0.2ns

Minimum value for t_{CLK} (ns): 6.2
or explain why none exists

$t_{CLK} \geq t_{PD,REG} + 2 * t_{PD,XOR} + t_{SETUP,REG} = 1.6 + 2*2.1 + 0.4$

(B) Using the same timing specifications as in (A), determine the setup and hold times for IN with respect to the rising edge of CLK.

$2 * t_{PD,XOR} + t_{SETUP,REG}$

t_{SETUP} for IN with respect to CLK↑ (ns): 4.6

$t_{HOLD,REG} - t_{CD,XOR}$

t_{HOLD} for IN with respect to CLK↑ (ns): 0.05

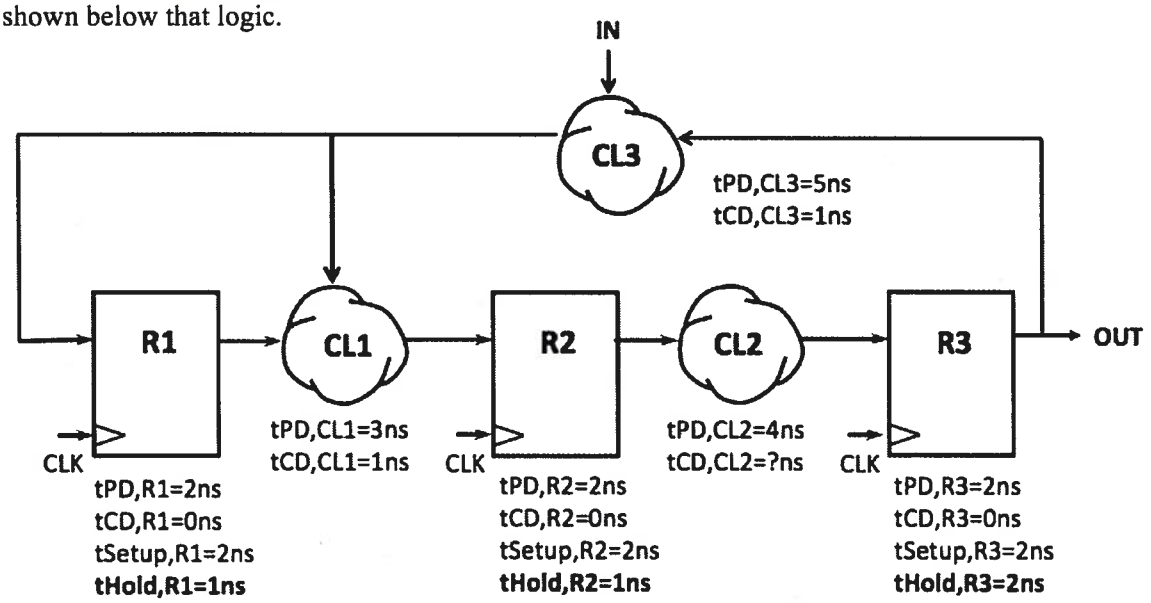
(C) One of the engineers on the team suggests using a new, faster XOR2 gate whose t_{CD} = 0.05ns and t_{PD} = 0.7ns. Determine a new minimum value for t_{CLK} or write NONE and explain why no such value exists.

Minimum value for t_{CLK} (ns): NONE
or explain why none exists

Now $t_{CD,REG} + t_{CD,XOR}$ is not greater than $t_{HOLD,REG}$

Problem 2.

Consider the following sequential logic circuit. It consists of three D registers, three different pieces of combinational logic (CL1, CL2, and CL3), one input IN, and one output OUT. The propagation delay, contamination delay, and setup time of the registers are all the same and are specified below each register. **The hold time for the registers is NOT the same** and is specified in bold below each register. The timing specification for each combinational logic block is shown below that logic.



(A) (1 point) What is the smallest value for the t_{CD} of CL2 that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

$t_{CD,R2} + t_{CD,CL2} \geq t_{HOLD,R3}$

$0 + ? \geq 2$

Smallest value for t_{CD} of CL2 (ns): 2

(B) (2 points) What is the smallest value for the period of CLK (i.e., t_{CLK}) that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

$(\sum t_{PD}) + t_{SETUP}$ R1→R2: 2+3+2 R3→R1: 2+5+2

R2→R3: 2+4+2 ~~R3→R2: 2+5+3+2~~

Smallest value for t_{CLK} (ns): 12

(C) (2 points) What are the smallest values for the setup and hold times for IN relative to the rising edge of CLK that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

longest path: $t_{PD,CL3} + t_{PD,CL1} + t_{S,R2} = 10$

Setup time for IN (ns): 10

shortest path: $t_{H,R1} - t_{CD,CL3} = 1 - 1 = 0$

Hold time for IN (ns): 0

(D) (2 points) What are the propagation delay and contamination delay of the output, OUT, of this circuit relative to the rising edge of the clock?

from R3

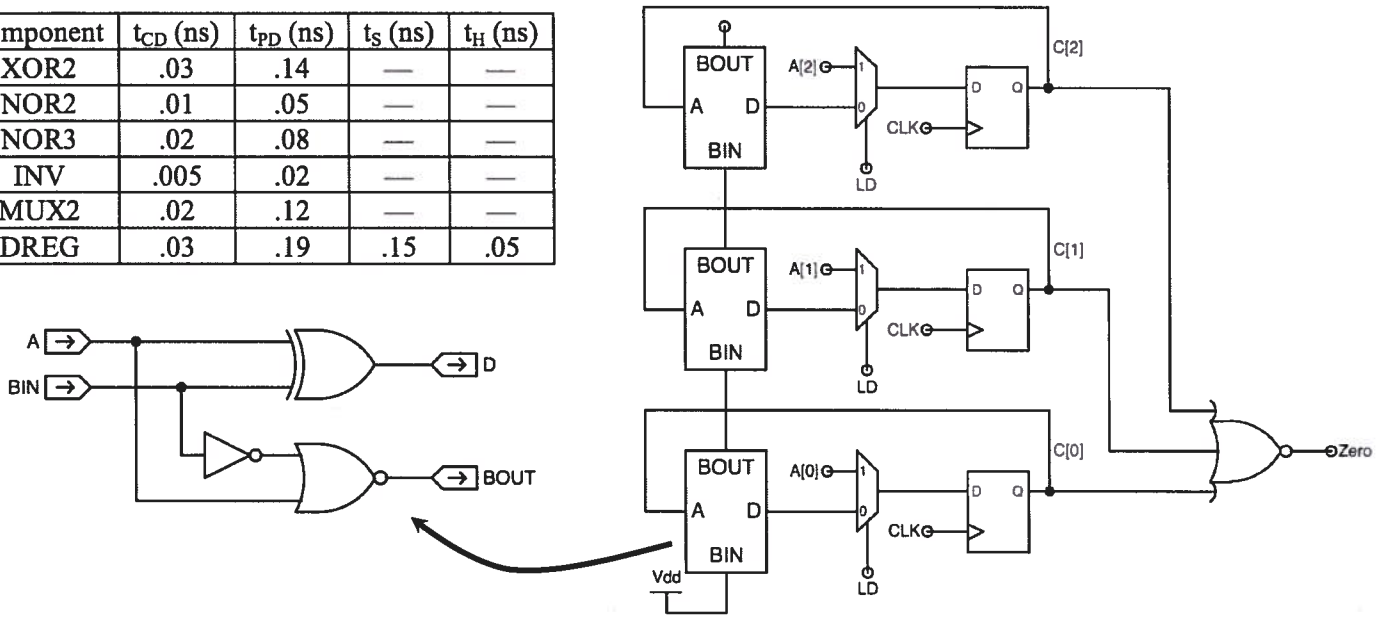
t_{PD} for OUT (ns): 2

t_{CD} for OUT (ns): 0

Problem 3.

Here's a schematic for a 3-bit loadable down-counter, which uses a ripple decrementer as a building block:

component	t_{CD} (ns)	t_{PD} (ns)	t_S (ns)	t_H (ns)
XOR2	.03	.14	—	—
NOR2	.01	.05	—	—
NOR3	.02	.08	—	—
INV	.005	.02	—	—
MUX2	.02	.12	—	—
DREG	.03	.19	.15	.05



(A) Using the contamination delays (t_{CD}), propagation delays (t_{PD}), setup times (t_S), and hold times (t_H) shown in the table above, please compute the minimum value for the clock period (t_{CLK}) for which the circuit will work correctly.

$(\Sigma t_{PD}) + t_{setup}$ along longest path **minimum value for t_{CLK} (ns):** 0.72

$t_{CLK} \geq t_{PD,REG} + t_{PD,NOR2} + t_{PD,INV} + t_{PD,NOR2} + t_{PD,XOR2} + t_{PD,MUX2} + t_{SETUP}$
$.19 \quad .05 \quad .02 \quad .05 \quad .14 \quad .12 \quad .15$

(B) What are the appropriate values for the setup (t_S) and hold (t_H) times for the **LD** input with respect to the rising edge of the clock?

$t_{S,LD} = t_{S,REG} + t_{PD,MUX2}$ $\quad .15 \quad .12$

setup time (t_S) for LD: 0.27

$t_{H,LD} = t_{H,REG} - t_{CD,MUX2}$ $\quad .05 \quad .02$

hold time (t_H) for LD: 0.03

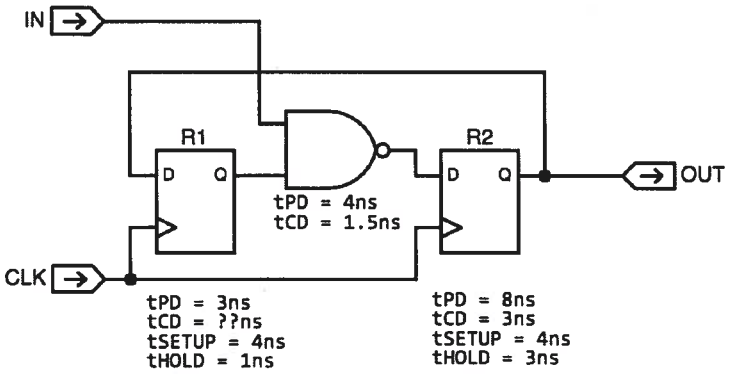
(C) What is the t_{PD} for the Zero output with respect to the rising edge of CLK?

t_{PD} for Zero (ns): 0.27

$t_{PD,Zero} = t_{PD,REG} + t_{PD,NOR3}$
$.19 \quad .08$

Problem 4.

Consider the following sequential logic circuit. The timing specifications are shown below each component. Note that the two registers do NOT have the same specifications.



(A) What are the smallest values for the setup and hold times for IN relative to the rising edge of CLK that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

$t_{S,IN} = t_{PD,NAND} + t_{SETUP,R2}$ (4 + 4)

Setup time for IN (ns): 8

$t_{H,IN} = t_{HOLD,R2} - t_{CD,NAND2}$ (3 − 1.5)

Hold time for IN (ns): 1.5

(B) What is the smallest value for the period of CLK (i.e., tCLK) that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

$t_{CLK} \geq$ { R1→R2: 3+4+4 = 11; R2→R1: 8+4=12 }

Smallest value for tCLK (ns): 12

(C) What is the smallest for the tCD of R1 that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

$t_{CD,R1} + t_{CD,NAND2} \geq t_{HOLD,R2}$ (? + 1.5 ≥ 3)

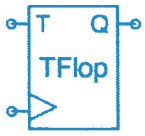
Smallest value for tCD of R1 (ns): 1.5

(D) Suppose two of these sequential circuits were connected in series, with the OUT signal of the first circuit connected to the IN signal of the second circuit. The same CLK signal is used for both circuits. Now what is the smallest value for the period of CLK (i.e., tCLK) that will guarantee the dynamic discipline is obeyed for all the registers in the circuit?

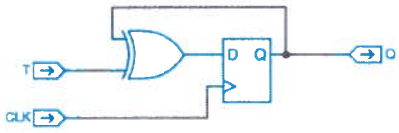
Smallest value for tCLK (ns): 16

$t_{CLK} \geq t_{PD,R2} + t_{PD,NAND}^{next} + t_{S,R2}^{next}$ (8 + 4 + 4)

Problem 5.



It is often useful to make clocked devices that count in binary, and a simple building block for such binary counters is the toggle flipflop whose symbol is shown on the right. It is a clocked device, hence the clock input indicated by the triangle on its lower-left edge. The other input, T (for *toggle*), may be set to one to cause the TFlop to flip its state (the *Q* output) from 0 to 1 or vice versa on the next active (positive) clock edge. If T is zero at an active clock edge, the state of the TFlop remains unchanged. We assume that the initial state of each TFlop at power-up is *Q=0*; more sophisticated versions might feature a *Reset* input to force a *Q=0* state.



A TFlop may be implemented using a D flipflop like the ones developed in lecture together with an XOR2 gate, as shown to the left.

As is our convention for clocked devices, we would like to specify timing specs for the TFlop as t_{CD}, t_{PD}, t_{SETUP}, and t_{HOLD}, all measured relative to the active (positive) clock edge.

(A) The timing specifications for the components are shown in the table below. Give appropriate values for the timing specifications of the TFlop implementation shown above.

Component	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
XOR2	40ps	400ps	–	–
DREG	100ps	300ps	80ps	40ps

$t_{CD,REG}$ **t_{CD}:** 100 **ps**

$t_{PD,REG}$ **t_{PD}:** 300 **ps**

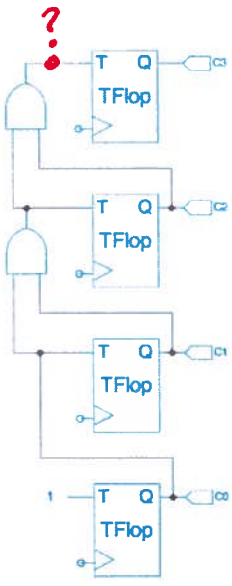
$t_{PD,XOR} + t_{S,REG}$ **t_{SETUP}:** 480 **ps**

$t_{H,REG} - t_{CD,XOR}$ **t_{HOLD}:** 0 **ps**

(B) Suppose we connect the T input of a single TFlop to 1 (i.e., V_{DD}) and try to clock it at its maximum rate. What is the minimum clock period we can use and expect the TFlop to perform properly?

$t_{CLK} \geq t_{PD,REG} + t_{CD,XOR} + t_{S,REG}$ (300 + 400 + 80)

***Minimum* clock period for correct operation:** 780 **ps**



We next consider the use of four TFlops to make a 4-bit ripple-carry counter as shown to the left. Assume that the TFlops share a common clock input (not shown) with an appropriate period, and that all TFlops have an initial Q=0 state.

(C) Suppose we run this circuit for a large number, N, of clock cycles. For approximately how many of the N active clock edges would you expect the T input to the topmost TFlop to be 1?

TOPMOST T=1 when C0 = C1 = C2 = 1 → every 8 cycles

***Topmost* T=1 occurrences in N cycles:** N/8

(D) If the AND2 gates have t_{PD} =200ps and t_{CD} =40ps, what is the minimum clock period we can use for the 4-bit counter?

***Minimum* clock period for correct operation:** 1180 **ps**

$t_{CLK} \geq t_{PD,REG} + 2 * t_{PD,AND} + t_{PD,XOR} + t_{S,REG}$ (300 + 2*200 + 400 + 80)

6.004 Computation Structures
Spring 2017