

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
 Department of Electrical Engineering and Computer Science

6.012 MICROELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 8

Issued: October 28, 2009

Due EARLIER than normal: 5 pm, Tues, Nov. 3, 2009

Reading Assignments:

- Lecture 14 (10/28/09) - Chap. 15 (15.1)
- Lecture 15 (11/3/09) - Chap. 15 (15.2.4)
- Lecture 16 (11/5/09) - Notes

Exam 2: Thursday, Nov. 5, 7:30 – 9:30, covering thru Lecture 15 and PS #8, including BJT operation and large signal modeling; the MOS capacitor; MOSFET operation (in strong inversion and sub-threshold) and large signal modeling; MOSFET inverters and CMOS; and incremental models for diodes, BJTs, and MOSFETs.

Note on this Problem Set: Most of the problems on this set originated in modified form as questions on prior exams, and have relatively short, quick answers. It may seem long at first, but it is not that bad, and as you work through it you will hopefully find yourself reviewing material that will be on the exam, i.e., studying for the exam.

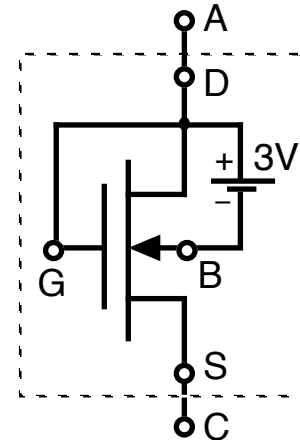
Problem 1 - This problem has two parts. Think of it as a warm-up for Hour Exam 2.

- (a) Consider two npn silicon bipolar junction transistors, A and B. All of the dimensions of these two devices, and the magnitudes of all of the doping levels in these two devices are identical, except that the base width, w_B , of Transistor A is twice that of Transistor B.
 - (i) Which transistor, if either, has the larger dc current gain, β_F ? Explain your answer and estimate the ratio of the two β_F 's.
 - (ii) Which transistor, if either, has the larger emitter-base junction saturation current, I_{ES} ? Explain your answer and estimate the ratio of the two I_{ES} 's.
 - (iii) With the base-collector junctions of both transistors reverse biased with the same values of base-collector junction voltage, V_{BC} , which transistor, if either, has the largest small-signal base-collector junction capacitance, C_μ ? Explain your answer and estimate the ratio of the two C_μ 's.
 - (iv) With both transistors biased at the same quiescent collector current level, I_C , which transistor, if either, has the largest small-signal transconductance, g_m ? Explain your answer and estimate the ratio of the two g_m 's.
 - (v) With both transistors biased at the same quiescent collector current level, I_C , which transistor, if either, has the largest small-signal input resistance, r_π ? Explain your answer and estimate the ratio of the two r_π 's.
 - (vi) Which transistor, if either, has a larger Early voltage, V_A ? Explain your answer.

- (b) This part involves MOSFETs.
- Consider two MOSFETs, one an n-channel MOSFET and the other a p-channel MOSFET. They have identical dimensions, and both are biased in the saturation region at the same drain current, $|I_D|$. Which of the devices, if either, would have the larger transconductance, g_{mV} and why?
 - Consider two MOSFETs, one an n-channel MOSFET and the other a p-channel MOSFET. They have identical dimensions, and both are biased in the sub-threshold region at the same drain current, $|I_D|$. Which of the devices, if either, would have the larger transconductance, g_{mV} and why?
 - An n-channel MOSFET operating in a circuit was mistakenly biased in the linear region. Derive expressions in terms of V_{GS} , V_{DS} , and K for its transconductance, g_{mV} and output conductance, g_o , in this situation. Assume $v_{BS} = 0$ and $\alpha = 1$, and ignore the Early effect, i.e., assume $\lambda = 0$.

Problem 2 - Consider the n-channel MOSFET circuit pictured to the right. The circuit is biased with $V_{AC} = V_{DS} = 2$ Volts. The MOSFET has following parameters:

$$\begin{aligned} K &= 2 \text{ mA/V}^2 \\ V_T &= 1 \text{ V} \\ \alpha &= 1 \\ \lambda &= 0.01 \text{ V}^{-1} \\ \eta &= 0.2 \end{aligned}$$



A small signal voltage, $v_{ac}(t)$, is added to the 2 V bias so now $v_{AC}(t) = 2 \text{ V} + v_{ac}(t)$.

- What are the bias and small signal values of v_{GS} , v_{DS} , and v_{BS} ?
- Use the linear equivalent circuit (LEC) for a MOSFET to draw the full LEC for this circuit. Evaluate all of the parameter values in your LEC.
- Reduce your LEC in Part ii) to a single element and give an expression for this element in terms of g_m and g_o .

Problem 3 - On Slide 8 in Lecture 14 the voltage gain of an NMOS inverter stage is calculated for the bias point $V_{IN} = V_{OUT}$, which is in the steep portion of the transfer characteristic. The substrate and source of the depletion mode pull-up MOSFET were shorted together, but this is not possible in many fabrication processes. Instead, the substrate of the pull-up MOSFET must be tied to ground. Redo the voltage gain calculation in this case by doing the following steps:

- What is the small signal base-to-source voltage, $v_{bs,pu}$ on the pull-up MOSFET?
- Draw the small signal linear equivalent circuit of the pull-up MOSFET. Notice that incrementally the drain is also connected to ground so that the substrate and drain are connected incrementally. Thus the pull-up MOSFET looks like a two terminal device in this connection and its LEC is simply a resistor (i.e., r_{pu} or g_{pu}). Give an expression for g_{pu} in terms of $g_{o,pu}$ and $g_{m,pu}$. (Remember g_{mb} and g_m are related.)
- Draw the LEC for the entire inverter; be sure to indicate v_{in} and v_{out} .

- (d) Derive an expression for the voltage gain, $A_v = v_{out}/v_{in}$, (i) in terms of $g_{m'}$, $g_{mb'}$, and g_o of the two transistors, and (ii) in terms of the bias point current and K , λ , and η of the two transistors.
- (e) Is the gain larger or smaller than when the pull-up substrate was tied to its source, or is it no different? Explain your answer.

Problem 4 - The gates on a CMOS logic chip were laid out by a designer who had not taken 6.012 and they have $W_p = W_{min}$ and $W_n = 2 W_{min}$, instead of $W_n = W_{min}$ and $W_p = 2 W_{min}$. What was the impact of this error on the following inverter performance metrics relative to the usual case of an inverter with $W_n = W_{min}$ and $W_p = 2 W_{min}$? State whether each has increased, decreased, or not changed appreciably, and explain your answers.

- (a) Inverter input capacitance, C_L .
- (b) The output node charging current after the input has switched from HI to LO.
- (c) The output node discharge current after the input has switched from LO to HI.
- (d) Static power dissipation.
- (e) The logic HI voltage.
- (f) The noise margins.

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