MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

6.331 Advanced Circuit Techniques

Spring Term 2002 | Issued : February 22, 2002
Problem Set 3 | Due : Friday, March 1, 2002

Problem 1 Consider the four-diode-switch sample and hold circuit:

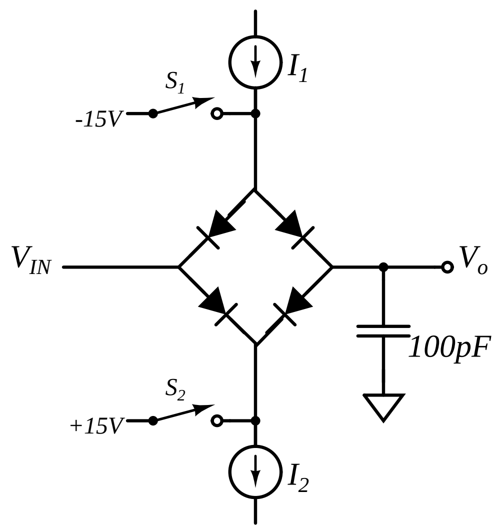

Figure 3.1: Four Diode Switch Circuit

In the sample mode, switches S_1 and S_2 are open, thus allowing the currents I_1 and I_2 to bias the diodes in the usual manner. In the hold mode, S_1 and S_2 are closed. Thus the diodes are reverse biased, insuring a rapid turn-off. This problem investigates the various sources of error inherent in this design. For each source of error, indicate whether it results in an offset error or a scale factor error.

(a) Let $I_1 = 10$ mA, $I_2 = 9$ mA. What is the maximum slew rate of the hold capacitor voltage in both the positive and negative directions? If the circuit is in equilibrium in the sample mode, what is the error caused by the given current imbalance? Use the diode model:

$$i_D = I_S e^{qv_D/kT} \qquad I_S = 10^{-13}\text{A}$$

(b) Assume that $I_1 = I_2 = 10$ mA. How long does it take for this circuit to slew 10 volts? Sample mode is ended when S_1 and S_2 close. If the switches don't close simultaneously, an error is introduced. Evaluate this error for the case in which S_1 closes 1 ns late.

(c) Assume that each diode is shunted by 10pF of stray capacitance. There will be charge dumped through this capacitance when the switches close. Evaluate the effects of this charge dump. Assume that all of the stray capacitances are equal, but the equilibrium output level was +5 V just before the switches were closed.

(d) Assume that $I_1 = I_2 = 10$ mA, and the circuit is in equilibrium in the sample mode. Consider the circuit's response to small changes in v_i. Use an incremental diode model. This analysis is valid as long as $|v_o - v_i|$ is on the order of kT/q. Compute the response to a step change in v_i. What is the 0.1% settling time? What is the response if v_i is a ramp?

Problem 2 Consider the following loop transfer functions:

$$L_1(s) = \frac{10^6}{s} \qquad L_2(s) = \frac{10^6}{s+1} \qquad L_3(s) = \frac{10^{10}(10^{-4}s+1)}{s^2} \qquad L_4(s) = \frac{10^6(10^{-4}s+1)}{(10^{-2}s+1)^2}$$

For each loop transfer function:

(a) Plot an asymptotic Bode Plot.

(b) Find the open loop DC gain, the crossover frequency ω_c, and the phase margin ϕ_M.

(c) Find the error transfer function, assuming that the above loop transfer functions describe op amp circuits with unity feedback.

(d) Find the steady state error to a 1 V step input.

(e) Use synthetic division to find the first three error coefficients of the error series, e_0, e_1, and e_2.

(f) For a unit ramp input, the steady state error grows as

$$e_{ss} = e_0 t + e_1$$

Find the steady state error e_{ss} to an input ramp with a slope of 1 V/μs. Comment on the relative magnitude and measurability of these errors.

(g) Use MATLAB to simulate (with `lsim`) the actual error response to the above ramp. Show and comment on the fast transient versus the slow transient.

Problem 3 An operational amplifier connected as a unity-gain non-inverting amplifier is excited with an input signal

$$v_i(t) = 5\arctan(10^5 t)$$

Estimate the error between the actual and ideal outputs assuming that the open-loop transfer function can be approximated as indicated below. (Note that these transfer functions all have identical values for unity-gain frequency.)

(a) $a(s) = 10^7/s$

(b) $a(s) = 10^{13}(10^{-6}s+1)/s^2$

(c) $a(s) = 10^{19}(10^{-6}s+1)^2/s^3$