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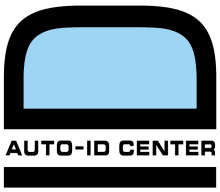

WHITE PAPER

Towards the 5¢ Tag

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ABSTRACT

Radio Frequency Identification (RFID) systems consist of readers, also called interrogators, and tags, also called transponders. This paper deals with RFID tags. Specifically, we deal with IC-based (integrated circuit based), passive, packaged RF tags with 64 bits of read-only memory. Today, tags cost upwards of 50¢, but there is great demand for low-cost RF tags. The specified target of 5¢ tags is theoretically unattainable with today's approach. The objective of this write-up is to describe the components of the RFID tag, and to explain how the cost of the system can be reduced to 5¢ tags.

RFID tags are themselves complicated systems, and the design of the optimal RFID tag requires the careful coordination of IC design, antenna design, manufacturing process engineering, and paper engineering. It is a careful system-level approach, combined with new technologies and new approaches that we describe here, that will enable low-cost RFID systems. Low cost RFID tags cannot be delivered by simply scaling up volumes while using existing technology.

The description presented here is speculative. First, research and development in RFID is an ongoing activity at the Auto-ID Center and its sponsors companies. As with any research activity, we can make some educated guesses about the possibilities, and back them up with engineering reasoning. However, we have not yet achieved that target. Second, some of technologies are confidential. We cannot therefore describe them in detail. However, we hope to convey the key ideas which we believe will enable the first 5¢ tags.

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Towards the 5¢ Tag

Biography

by Sanjay Sarma
Research Director

Sanjay Sarma received his Bachelors from the Indian Institute of Technology, his Masters from Carnegie Mellon University and his PhD from the University of California at Berkeley. In between degrees he worked at Schlumberger Oilfield Services in Aberdeen, UK, and at the Lawrence Berkeley Laboratories in Berkeley, California. Dr. Sarma's Masters thesis was in the area of operations research and his PhD was in the area of manufacturing automation. From 1995 to 1999, Dr. Sarma was an assistant professor in the Department of Mechanical Engineering at the Massachusetts Institute of Technology. He is now an associate professor.

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Towards the 5¢ Tag

Contents

1. INTRODUCTION

Radio Frequency Identification (RFID) systems consist of readers, also called interrogators, and tags, also called transponders. This paper deals with RFID tags. Specifically, we deal with IC-based (integrated circuit based), passive, packaged RF tags with 64 bits of read-only memory. Today, tags cost upwards of 50¢, but there is great demand for low-cost RF tags. The specified target of 5¢ tags is theoretically unattainable with today's approach. The objective of this write-up is to describe the components of the RFID tag, and to explain how the cost of the system can be reduced to 5¢ tags.

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2. THE ANATOMY OF AN RF TAG

An IC-based RF tag consists of the four components:

1. the IC,
2. the antenna,
3. the connection between the IC and the antenna, and
4. the substrate on which the antenna resides.

In supply chain applications, tags themselves are usually attached to a package or to a container. A schematic of an RFID tag is shown below.

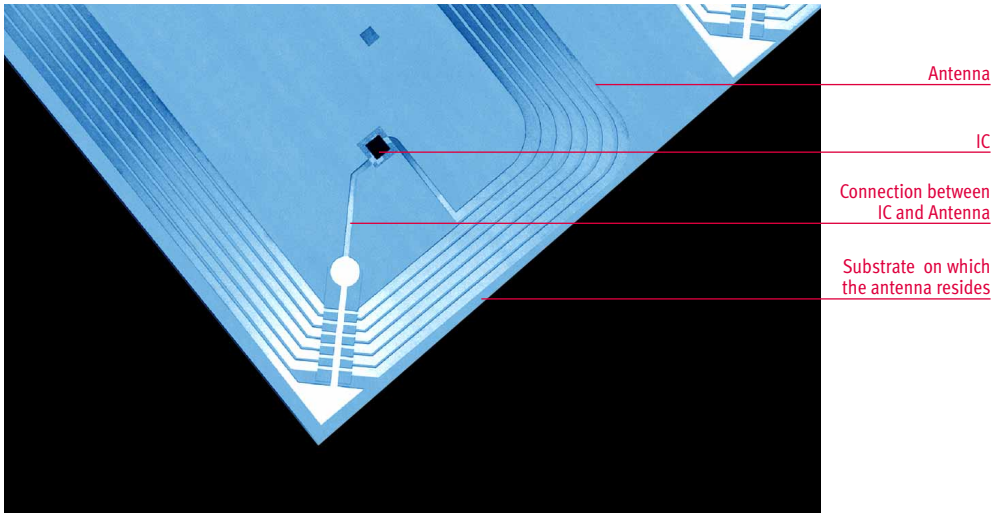
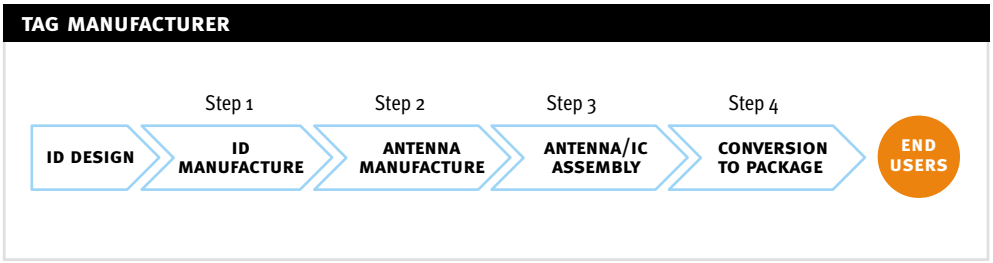


Figure 1: Courtesy Rafsec OY (OY means Co. in Finnish)

Figure 2



After the design of the IC, there are four steps in the manufacture of an RFID tag, as shown above.

– **The first step** is the manufacture of the integrated circuit, or IC.

– **The second step** is the manufacture of the antenna. The antenna is a conductive element shaped to a specific configuration.

– **The third step** is the assembly of the IC to the antenna. In fact this step has two sub-parts:
a) the placement of the IC in a specific location with respect to the antenna, and
b) connection of the electrical contacts on the IC with the ends of the antenna.

– **The fourth step** is the conversion of the antenna, with the IC attached, first to substrate, and then to a package.

Each of these steps is a challenge, and the costs of all these steps must add up to less than 5¢. The cost budget for each of these steps is in the order of 1¢ (Lindstrom 2000). This is obviously a challenging task. Today, the IC costs 20¢, the antenna, the assembly and the pre-conversion cost about 5¢ each, and the conversion often costs more than 10¢.

These cost budgets have profound implications for every component of RFID technology. Consider IC manufacturing. The cost of a 200mm wafer is in the range of $1,000. The per-mm^2 cost of finished silicon, with overhead of the spacing between individual chips, is about 4¢. A 1–2¢ budget tells us that the size of silicon for the IC must be in the range of 0.25mm^2, or about 0.5mm on the side. Yet this size is very difficult to handle with conventional IC fabrication techniques. Challenges such as these have confounded the RFID industry over the last few years. The vicious cycle of cost, size and demand can only be disrupted by an approach which seeks and harnesses synergies in the larger system, and at the same time, employs the latest technology for each component.

3. THE SYSTEM

The first step in reducing the size of the IC is to minimize the functionality required on the IC. As stated above, the size of the IC cannot exceed 0.25mm^2. This goal is impossible to achieve without an approach which encompasses every aspect of the RFID system. The first step we must undertake is to transfer as much functionality as possible from the IC to the back-end system. Essentially, this is equivalent to reducing variable costs in the system at the expense of fixed costs. Economically, this makes sense; given the huge volumes of tags we expect, the variable cost must be minimized. The table below summarizes the numbers of tags that would be consumed by our sponsors alone if they chose to tag every item they produced.

Table 1: *denotes Auto-ID Center estimate. All others sponsor estimates

END USER	ESTIMATE NO. OF UNITS IN SUPPLY CHAIN (BILLIONS)
CHEP	0.2
JOHNSON & JOHNSON consumer goods division	3.0
KIMBERLY CLARK*	10.0
WESTVACO*	10.0
THE GILLETTE COMPANY	11.0
YFY*	15.0
TESCO	15.0
THE PROCTER & GAMBLE COMPANY	20.0
UNILEVER	20.0
PHILIP MORRIS GROUP*	25.0
WAL-MART*	30.0
INTERNATIONAL PAPER	53.0
COCA-COLA*	200.0
SUB-TOTAL	**412.2**
(Adjust for double counting @15%)	– 61.8
United States Postal Service	205.0
TOTAL INCLUDING USPS	**555.3**

In this section we describe the software and algorithmic decisions taken to minimize the functionality of the RFID tag. There are three major contributors to the area on a chip: the memory, the logic, and the power circuitry. Section 3.1 summarizes material first presented in a previous document (Sarma et. al. 1999) where we described a software system designed by the Auto-ID Center. This system reduces the memory requirement on the chip. In Section 3.2 we describe the logic on the chip, and how we have minimized it. In Section 3.3, we describe the power circuitry.

3.1. Memory on the Chip

We address the memory limitation with two concepts: the EPC and the ONS.

The EPC

We employ a numbering scheme called the electronic product code (EPC) to **point at locations on the network** where we store information. The EPC consists of four fields: the version number, the manufacturer number, the product number and a unique serial number for each individual tag. The tag itself only stores the EPC, which, depending on the version number, is 64 or 96 bits long. This is a primary tenet of our system. By requiring the tag to have nothing more than the EPC, we achieve two functions. First, we limit the memory on the chip. Second, we reduce the minimum requirement of the system to read-only tags. Read-only memory has a much smaller footprint than non-volatile memory.

Does this approach not limit the system? The answer is no. In fact it enhances the amount of information that can be stored in reference to an object, and makes it more secure. We explain below.

A mapping service called the Object Name Service (ONS) maps the EPC to an IP (Internet Protocol) address where information that one desires to store about the tag can be written and accessed. The ONS is based entirely on the Domain Name Service (DNS) which is a very well known mapping service used on the Internet today to map a domain name like www.mit.edu to an IP address like 18.181.0.31. At the IP address pointed to by the ONS, data about the particular EPC is stored in XML format, and can be accessed by standard methods like HTTP and SOAP. The redirection service reduces the burden on the tag, and achieves several purposes simultaneously. First, it reduces the space and power requirements on the tag. Second, by transferring much of the data communication to a much higher-bandwidth back-end network, it saves precious wireless bandwidth. Third, it makes the system more robust: while it is difficult to store and recover information from a failed tag, it is possible to back up databases inexpensively.

3.2. Logic on the Chip

The logic in our simple chip need deal with one problem primarily: reading multiple tags. While the issues are too complicated to be described in any detail in this article, the important points can be summarized briefly. When many tags are in the reader's field, it is necessary for the reader to sort their responses into collision-free channels. This is referred to as tag anti-collision. There are a great number of anti-collision algorithms available, each optimal for different regulatory and functional requirements. In our case, where tags carry the structured EPC numbering scheme, only two functions are necessary: the ability to rapidly read several tags, and the ability to rapidly bit-mask the search down to certain version, manufacturer or product numbers. In doing so, the anti-collision scheme must be implementable on a minimal amount of silicon. The anti-collision scheme developed by the Center and its sponsor companies is optimized for size and speed.

3.3. Power Circuitry

Finally, the size of the IC also depends on the power circuitry on the chip. A principle component of this circuitry is the capacitor, which stores energy on the chip to permit operation without a battery.

A synergistic effect of our approach is that it minimizes the power requirement of the tag. Therefore, the power storage capacitor need not be large at all.

3.4. Summary

In summary, we have designed a system that minimizes the required size of the chip. This is the first step in achieving our goal of a 5¢ tag. In addition, this system offers a number of advantages such as security, integrity, speed and scalability. The remainder of the challenge is in the manufacturing of low-cost IC's and low-cost tags.

4. IC MANUFACTURING

In the section above, we have described how to minimize the size of the IC, thus minimizing silicon cost. The target size of the IC is now 0.5mm on the side or less. This target size, however, raises new issues related to handling costs. While Moore's Law predicts an exponential drop in packaging cost over time, ancillary costs will actually flatten out and become the dominant component of the cost budget if currently available commercial technology is used. Ancillary costs include handling costs, testing costs and the cost of silicon wasted in dicing (these strips are referred to as "streets.") We address these questions in this section.

4.1. The Manufacture of IC's

It is useful to consider the process by which silicon integrated circuits are typically manufactured today.

4.1.1. Wafer Preparation

IC fabrication starts with the production of silicon ingots. Ingots are created by growing a silicon crystal around a "seed" – an element of perfect crystal around which the growing crystal aligns itself naturally. Today, ingots need to be over 300mm in diameter, several feet in length, and several hundred pounds in weight. Second, the ingot is shaped and sliced into wafers. These slices are usually in the range of 1mm in width. Slicing is done by one of two methods: by an annular saw or by cutting with wires. The output of this stage is a wafer: a flat, circular segment of silicon. This wafer must now be polished and treated before circuit fabrication can begin. The sub-steps at this stage are lapping, etching, beveling, double-sided lapping, chemical etching, annealing, fine polishing and wet-cleaning. The result of these operations is a smooth wafer with very high surface flatness.

4.1.2. Wafer Fabrication

The production of the wafer enables the next step of IC manufacture: the lithography stage. Circuits are laid down by a series of additive and subtractive processes. Addition is done in many ways depending on whether the material being added is an insulator, an alloying element, or a conductor. Subtraction is carried out by exposing the wafer to an acid, a base or some other corrosive environment, and this is usually referred to as etching. The control of which region is undergoing what process is achieved by masking: a material known as photoresist is spin-coated over the planar wafer to cover the evolving circuit. The photoresist is exposed to a pattern of light from a light source above. The exposure pattern is created by passing light through an optical stencil called a mask or a reticule. The areas exposed to light harden, and the rest of the photoresist can be washed away. The areas not covered by the photoresist can now be processed by either the additive process, or by the subtractive process. A typical wafer may go through hundreds of such cycles to lay down the ultimate circuit.

Finally, once the silicon has been patterned, the next step is to test it. Testing has traditionally been used for two reasons. First, to ensure that the IC works, and second, to monitor the process in real-time, so that process problems can be fixed immediately without affecting the yield. Testing is carried out by mechanical probes which make contact with areas in the circuit, transmit test signals, and validate the response of the circuit.

Several informal metrics are used to describe the complexity of the chip or the manufacturing process used to make it. One measure is the number of transistors, which are the basic valve in the plumbing that forms a silicon circuit, in the chip. The Pentium III Coppermine chip has 28 million transistors. Sometimes, the term "gate equivalents" is used. The number of gate equivalents is about a fourth of the number of transistors. Often, the complexity of the process is expressed in terms of the number of a special type of layer called the metal layer. Typical large-scale integrated circuits, such as those in the

Intel Pentium, have several metal layers. The Coppermine has 6 metal layers. Another measure is the size of the smallest feature in the IC. The smaller the feature, the greater the speed, the lower the power consumption, and the lower the cost per IC. The Coppermine was made using the Taiwan Semiconductor Manufacturing Company 0.18µm process. Finally, the cost of the IC is inversely proportional to the area of the IC. The Coppermine IC itself was 106mm^2 in size.

4.1.3. Packaging

After testing, the wafer goes to the next step: dicing and packaging. The first step is chips separation. This is usually preceded by first placing the wafer on an adhesive trampoline-like membrane for support. Next, scribe-lines are created on the IC. There are two ways to do this. The first approach, which works for thin wafers, is called scribing. A diamond tipped tool is used to create a groove about one third the thickness of the wafer. The wafer is then cracked along these scribe lines by stressing it between a pair of rollers. Unfortunately, for thicker wafers this approach has the potential problem of cracks which propagate into the active area of the die. A more recent approach is scribing with a diamond saw. This approach has the problem of requiring a significant width. The width of these cuts, which must be accounted for by leaving gaps (also referred to as streets) between adjacent dies, is in the order of 100µm.

The separated dies are now ready for packaging. Robots are usually employed to pick the dies up using vacuum chucks. In conventional IC's, the dies are bonded onto a frame called a lead-frame with the electric contacts facing upwards. Wires are then bonded from these exposed contacts, or pads, on the die, to the leads of the package. These leads connect the contacts on the silicon to the outside circuit, which is usually a printed circuit board. An alternative to wire-bonding is a family of techniques collectively known as flip chip. In these techniques, the die is made so that the pads have bumps on them. The die is flipped over and contacted directly into the leads. The area between the die and the frame is then filled with a polymer or epoxy.

Figure 3: Wire-bonding beads on the pads of an IC wire-bonding process Wire-bonding: Courtsey: http://www.eccb.org/pbps/tg/wirebond.htm, Bob Thomas, Ph. D., Technology Experts Network

4.2. How Costs Scale with Die Size

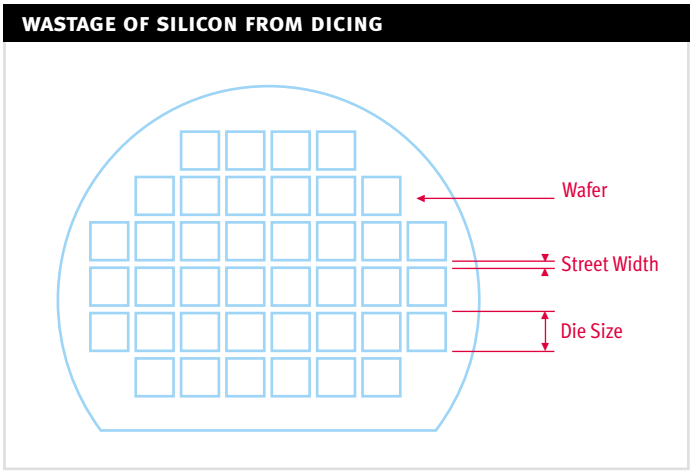
The techniques described above have evolved over the years to satisfy the needs of the conventional silicon industry. There are two counterbalancing trends in play. First, the complexity of circuits in IC's has increased exponentially to keep track of rapidly increasing demands on functionality. Second, as Intel founder Gordon Moore predicted in the seventies, the number of gates that can be built into a given area has doubled every 18 months. Interestingly, these two trends balance each other; as the size of gates has gone down, the number of gates required in the circuit has gone up. The result of this balance has been that the size of the IC for most applications has effectively remained constant over the years. Consider the Pentium, for example. In going from the older version of the Pentium III to the newer Coppermine version, the line width went from 0.25mm to 0.18mm, and the number of metal layers went from 5 to 6. This should have reduced the size of the chip, if functionality were kept constant,

by more than 50%. However, the Coppermine was only 15% smaller. This is because the number of transistors nearly tripled to keep track of the demands of the PC customer.

This balancing effect has effectively hidden an exception to Moore's trend. When IC's become small, dicing and handling costs do not scale with size. In fact they stay the same or actually increase on a per-IC basis. Yet, from our discussion in Section 2, we realize that this is precisely the challenge that RFID poses. Unlike other circuits, instead of adding functionality, we seek to reduce functionality so that the size of the IC is minimized. We explain these hidden costs below.

Figure 4

WASTAGE OF SILICON FROM DICING



Wastage of Silicon from Dicing

As described in Section 4.1.3, separation of wafers into dies is usually done with diamond saws. The streets created by these cuts are 100µm in width. Unfortunately, as the die becomes smaller, a greater percentage of the original silicon is wasted in streets. For example, if the die were 100µm on the edge, 75% of the wafer would be wasted, effectively defeating the purpose of migrating to a smaller die. The only way to address this problem is to eventually eliminate the diamond-saw operation in favor of other die-separation techniques that permit smaller streets.

Die Testing

When the number of dies increases to the extent that we foresee when the wafer is about 500mm on the edge, testing costs could begin to balloon. Already, testing can add $500 to a wafer. Testing equipment can cost about $500 per hour, and testing 60,000 wafers in an hour requires about thousand tests a second. This is a very demanding requirement, one that could stymie the effort for a low-cost IC. Later, we examine the reasons why we testing is done, and propose a radical approach.

Handling Costs

There are two reasons why handling costs do not necessarily scale with silicon costs. The first reason is because of the time it takes a robot to pick a die up from a wafer and place it on a carrier is independent of the size of the wafer; after all, the weight of the die is not the dominant or limiting factor in this process – it is the size of the robot itself that limits this process. Second when the die becomes small, the precision requirements on the vacuum chuck device may actually **increase**. Misalignment of this chuck may lead to a die that is picked up in "diamond mode," **i.e.**, with a corner pointing up into the vacuum chuck. Smaller dies require greater precision, and more precise robots usually cost more money unless carefully designed. Today, the practice is to purchase off-the-shelf machines and to shoe-horn RFID into existing IC manufacturing facilities. This is sub-optimal. Fortunately, better handling techniques have been developed, as have more economical assembly systems. We will describe them later.

Die-Connection Costs
Wire-bonding techniques scale with the number of pads on an IC. The RFID chip need only have two pads. Wire-bonding, if properly engineered, is therefore a potentially efficient process for RFID. However, the issue that arises is one of throughput. In order to meet the volumes necessary, RFID will probably require roll-to-roll manufacturing. Standard wire-bonding does not scale very well over size because each site undergoing an operation in parallel requires an individual wire-bonding head. Flip-chip techniques have found greater use in RFID systems. However, flip-chip techniques require expensive conductive pastes and often, longer dwell times for heat treatment. Therefore, neither process can be applied directly to RFID. However, as we will describe later, modified versions of these processes may be capable of meeting our needs.

Summary
In summary, it is important to keep in mind the fact that **RFID is different from standard IC's. "**Shoe-horning**"** RFID into existing manufacturing flows is sub-optimal, and it comes as no surprise that today's RFID systems are relatively expensive. Conventional wisdom has largely depended on the conventional rules quoted by today's silicon industry. Instead of treating the unique features of RFID technology as obstacles, it is advantageous to build a new system which harnesses them as advantages. The principal distinguishing features of the RFID IC's are:

1) they need to be very small, in the range of 500µm x 500µm;
2) they have only two pads; and
3) they will need to be very thin to permit conversion to consumer good packaging.

5. LOW-COST RFID

In this section we describe technological options available to reduce the cost of RFID chips in view of the pros and cons described in Section 4. In sequence, we address the challenges of cost-effective thinning, dicing, die handling, and electric connections. We also briefly describe antenna manufacturing and packaging.

5.1. Die Testing

As explained earlier, testing is performed for 2 reasons:

1. to monitor and adjust the process, and
2. to verify that the chip works.

The monitoring functionality can be achieved by testing a fraction of the dies, and is in fact a relatively inexpensive component of the cost equation. It is the functional verification that requires a testing of the full population. Our solution to this is simple: eliminate full testing. Instead, perform the testing action wirelessly after the RFID has been manufactured. There is a fundamental mechanical reason for this. Testing today uses probes at the end of a mechanical motion system. It is this mechanical motion that is likely to be the bottleneck in throughput when the numbers of dies is very large. Wireless testing, which is conveniently available in RFID, eliminates this problem. Since the RFID chip we are designing is very simple, the yield will tend to be high after the process is tuned. Furthermore, the anti-collision scheme that we have developed is very rapid when the distribution of EPC codes is serial. The read rates expected are in the range of several hundred a second. In addition, the cost of the testing equipment will be very low.

Another question that arises is where the testing should occur: at the label manufacturers location or at the location where the final packaging and conversion is done. We recommend that the testing actually be done at the final packaging stage. If the tags are write-once-read-many (WORM), the EPC code will actually be written at the final packaging step. Testing is most efficient when carried out at that point. The process would work as follows: the tags can arrive at the facility on rolls with adhesives on the back; prior to application, a tag can be singulated and the EPC written to it; the tag can then be tested, and discarded if it is faulty; and finally, if the tag works, it can be applied to the package. The writing and testing equipment is not likely to be expensive. The equipment for discarding faulty tags can also be very simple. This will result in significant cost savings on the whole.

5.2. Narrow Streets and Thin Wafers

Several new wafer-processing techniques have emerged in the last few years, and there are significant benefits which can be brought to bear on RFID. In combination, they enable thinner IC's and narrower streets. Thin wafers yield thin IC's, which in turn are easier to package in RFID tags. Smaller streets cause less wastage of silicon, and therefore lower costs.

First, consider thinning. The terms back-lapping, or back-grinding, refer to the removal of material from the rear of a wafer. Advances in grinding, chemical-mechanical polishing and wafer handling have made it possible to thin wafers much more economically than before. The process flow is as follows. After wafer fabrication, the active side of the wafer is covered with either a tape or a coating of polymer. The wafer is then turned upside down and ground on the back-side. If the desired wafer thickness is less than 100µm, the wafer may have to be mounted using a double-sided tape or adhesive on a carrier to prevent bending. Total thickness variation (TTV) after grinding can be in the range of 0.5 ~ 2µm for 150mm wafers. The ground surface is then finish-machined using a chemical polishing step or an etching step; this final step produces fine finishes without embedding residual stresses in the wafer, and also does not cause bending in extremely thin wafers. Wafers can now be thinned to a few 10's of micrometers. More information about wafer thinning is available in a number of publications such as (Müller **et. al**. 00) and (Hazeldine 01).

Now, consider etching. In traditional wet etching, it is often difficult to control the direction of the etch and to achieve narrow but deep trenches. Dry etching techniques, such as reactive ion etching (RIE) and sputter etching, permit deeper, sharper etches. In fact the process of deep reactive ion etching can achieve aspect rations of 50:1. A comprehensive background on the etching is available in (Rossnagel 90). Wet etching too has recently seen significant improvements. For example, Mitsubishi (MITSUBISHI) report 60:1 aspect ratios in wet-etched trenches. The costs of etching have also dropped significantly over the years, making large scale application more economical. The question that can now be asked is: can deep etching be used to separate dies with very narrow streets? The answer is "yes."

By combining wafer-thinning and etching techniques, it is today possible to separate dies from a wafer with very small street widths. The street widths achievable with this procedure are as small as 5µm instead of the 100µm that conventional saw-dicing techniques need (Landsberger **et. al**. 01). The process flow is as follows. The wafer is first etched from the front side using dry or wet etching to create deep grooves. The wafer is then back-ground. Final die-separation is achieved simply by a final chemical mechanical polishing step. This approach yields narrow streets, but also offers another significant advantages:

1. it permits cost-effective die-separation because it is a mass separation process; and
2. it produces smaller kerfs, and consequently, higher quality dies.

5.3. Die Assembly and Contact

Once the dies have been manufactured, they must be accurately to a substrate. In the IC industry, this is done in two stages. First, the dies are placed on lead frames. Next, the lead frames are turned into packages, and then assembled to the printed circuit board. RFID is usually manufactured similarly. Typically, the die is attached to a small substrate patch which creates the interconnection from the pads on the die to larger contacts on the patch. These patches are variously referred to as interposers, straps or carriers. These interposers are then attached to the antennas to create "inlets". Inlets are then converted to packaging. The first of these steps is the most difficult because it needs the greatest precision and speed. If the IC can be placed inexpensively and rapidly on a roll of interposers, then the second stage can similarly be carried out on a roll-to-roll process. Roll-to-roll processing is a key to inexpensive RFID manufacture. There are in fact several viable approaches, which we describe below.

5.3.1. Fluidic Assembly

In 1995, researchers at the University of Berkeley proposed a powerful new technology called Fluidic Self Assembly (FSA) for assembling very small IC's to substrates (Verma et. al. 95, Chiang 00.) In recent years, this technology has been spun-off to a startup company which claims the capability of roll-to-roll production of RFID interposers (Jacobsen 01). The method works as follows: after wafer fabrication, dies are parted from the wafer using wafer thinning, followed by a form of etching. The etching is carried out such that the dies emerge with a trapezoidal shape – referred to by Alien Technology as Nanoblocks™. Matching trapezoidal holes are meanwhile embossed into the substrate. The dies are suspended in a fluid, usually an alcohol solution, and then flowed into the embossed holes in the substrate. The process promises high yield and low costs, and importantly, the ability to scale to massive volumes. Perhaps most significantly, the fact that this process works in roll-to-roll mode is a very major step towards low-cost tags. Recently, Alien Technology has launched pilot project to develop dedicated RFID manufacturing machines based on this technology.

Once the dies are in place, interconnection to interposer leads can be carried out by a variety of techniques ranging from lithography to silk-screen printing. Several new partnerships are being developed around this technology between Alien Technology and other sponsors of the Auto-ID Center.

5.3.2. Pick-And-Place Assembly

New processes like fluidic self-assembly offer great promise However is important to note that though commercially available pick-and-place systems may not be capable of the through-put required for RFID, dedicated pick-and-place machines designed **for** RFID may well be able to meet the through-put requirements. The key observation is that because the RFID IC has only two contacts, pick-and-place and interconnection operations can be combined into a single step that can operate in a roll-to-roll configuration. Unlike in conventional IC's the extra step of die-bonding is not necessary in RFID. It is possible to speculate about machines that take advantage of these facts. For example, one instantiation would be for the IC to be picked from from the back using a vacuum chuck, and then placed on the inner leads of the interposer. Adhesion and electrical contact can be achieved using a conductive polymer glue or some other flip-chip mode of connection. The inner-leads themselves could be attached to a metal carrier frame, and could ride on a roll. This system would require a relatively inexpensive machine, and could potentially offer the necessary throughput for mass-scale, inexpensive manufacturing. Once the IC is attached to this roll of carriers, it is possible to perform other processes in a scalable way.

5.3.3. Vibratory Assembly

At MIT, we are developing a purely vibratory approach to delivering IC's to a substrate. Based on the principle of a vibratory bowl feeder, the system is being designed as a "chip-on-demand" dispenser. A 300Hz vibration is used to march the chips down channels and detents are used to order, orient

and align the chips. A larger demand-pulse is used to deliver the chip precisely when it is necessary to a roll of substrate material. The system is currently in prototype phase. Once the die is delivered, interconnection between the die and the interposer can be achieved in a number of ways which are similar to those for fluidic self-assembly.

5.3.4. On-Wafer Processing

Another very interesting process that has recently emerged is the idea of doing most of the processing directly on the wafer (Plettner 2001). At the Fraunhofer Institute and at FlexChip AG, besides developing expertise in thinning and dicing as explained earlier, the focus has been on eliminating much of the handling that needs to occurs after the die is separated. The result is a shift towards batch processing and away from the handling of single chips with the objectives of reducing machine time and lowering costs. The processes are also aimed at delivering very high reliability of the finished smart label with inherent physical and electrical advantages over labels produced using flip chip processes. One approach is to attach contact-elements, or inner leads, directly to the dies while the dies are still on the wafer using a flip-chip type of conection. These leads can effectively act as interposers, and are expected to allow large-scale integration of the IC's into RFID packages. The attachment of dies to inner leads can be carried out by a number of techniques including screen-printing as explained earlier. Figures below show a polymer contact and a lamination from (Feil **et. al**. 01).

Figure 5: Thinned die with polymer contact Courtesy: Fraunhofer Institute and FlexChip AG

Silver

Figure 6: Lamination Courtesy: Fraunhofer Institute and FlexChip AG

One of the issues that often comes up with flip-chip techniques is the cost of conductive polymers. Today, these materials may by themselves amount to about 0.5¢ per pad. However, these costs are usually computed based on low volumes and high margins. We speculate that these costs can be significantly reduced in high volumes. Secondly, several companies today offer conductive polymers that are significantly cheaper than traditional vendors (Estes 01).

5.4. Antenna Manufacturing and Attachment

RFID antennas are usually made by winding 30µm coated wire. The coil is then spot-welded directly on to the interposer (Finkenzeller 99). This procedure works in low volumes, and when cost constraints are not as severe; however, this procedure does not scale to high throughputs.

In response, several alternative technologies have been proposed and developed. They include conductive ink/paste printing, etching of copper wires, rolled metal antennas and other additive processes (Lindstrom 01). The trade-offs are between cost and quality. At high frequencies, for example, the quality factor requirements are lower, and there is more flexibility in the manufacture of the antenna. At low frequencies, conduction needs to be higher and the quality needs to be higher. Unfortunately, much of this research is outside the public domain at this point. However, our analysis of technologies under development with Auto-ID Sponsor companies has led us to the belief that the cost targets for antenna manufacturing are achievable.

5.5. Summary

Conventional silicon manufacturing technologies do not necessarily scale to the high-volumes and low costs necessary for item-level RFID tags. A number of inventions and innovations seem to have gone largely unnoticed by the RFID Industry over the last few years. However, in conjunction with the appropriate use of network and data-basing concepts, these technologies create a new pathway for low-cost tags.

6. SCALING ISSUES

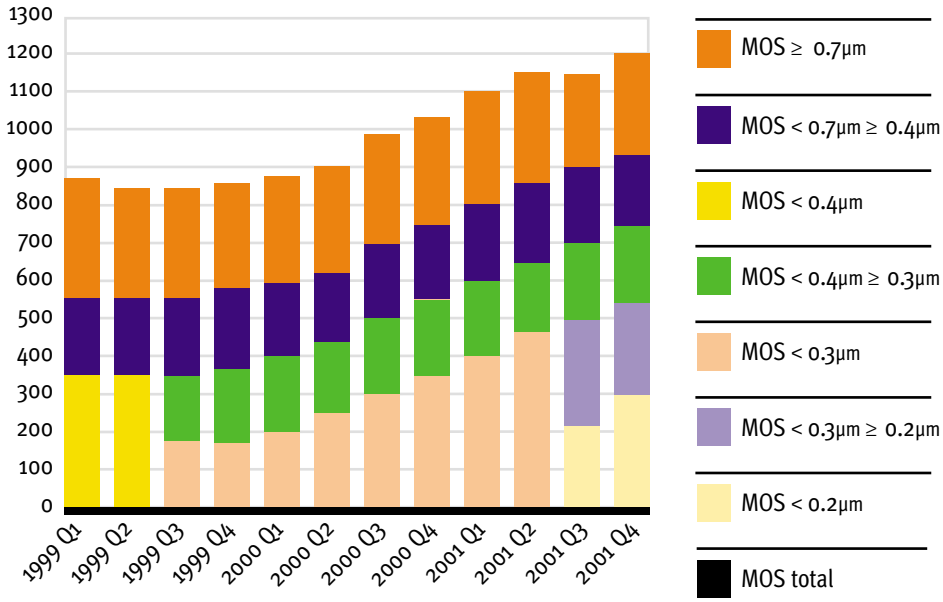
A primary goal of the Auto-ID Center is to make 5¢ RFID tags possible, and to lead the development of the first prototype which, at medium volumes, will scale to this cost target. However it is important to understand that this goal does not guarantee the immediate availability of 5¢ tags in large volumes. The economics of RFID tags and demand are interesting. Today, tags cost about 50¢ or more, and the total world-wide demand for tags at this cost is estimated to be about 400 million tags per year (Sharp 01). At 5¢, our research shows that total demand will be explosively larger. At about 1¢, the demand for RFID tags may well equal that for bar codes. The achievement of the 5¢ goal will therefore likely create a new problem hitherto unknown in the RFID community: **production capacity limits**.

Consider, for example, the UCC/EAN bar code. Currently, 5 billion bar codes are scanned world-wide every day. If the sponsors of the Center were to decide today to place tags on every item they manufacture, demand for IC's among sponsors alone could run to several hundred million tags a day. As a comparison, consider the world fab capacity for silicon wafer manufacturing. Today, daily fab capacity is about 1.5×10^5 wafers in terms of 200mm wafer-equivalents (Semichips 01). Growth is about 10–15% per year, as shown below. Even with high yields, this is equivalent to about 3–4 billion tags a day. Clearly, a significant fraction of the world fab capacity would become necessary to meet demand if adoption is very high.

Figure 7:
Note: All data in the graph are expressed in 8 inch equivalent wafers. The line "Total IC's" in the table includes the "Bipolar" data, which were converted for this purpose from 5 inch to 8 inch equivalent wafers by using the factor 0.391.

Source: SIA/SICAS, http://www.semichips.org /stats/xls/capq2_2001.xls

IC WAFER – FAB CAPACITY IN WAFER STARTS PER WEEK X 1000



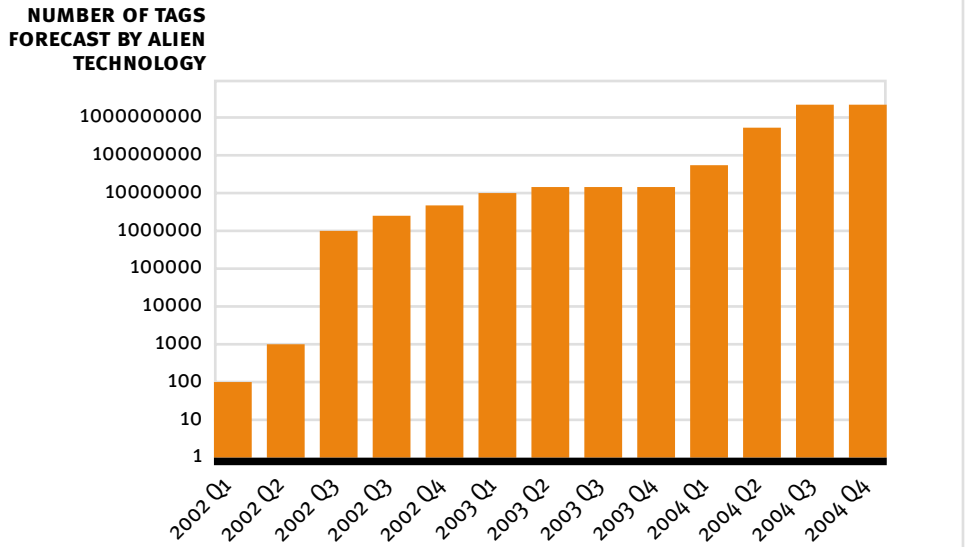
8 inch wafers in MOS TOTAL	
BIPOLAR	(5 inch equivalents)
Total IC's	**(8 inch equivalents)**

The other issue is one of ramp-up. In order to manufacture tags in large volumes, as described in this paper, new manufacturing processes will need to be developed, new machines fabricated, and the new suppliers lined up. This process too will delay the availability of large volumes of RFID for several years. As an illustration, we provide Alien Technology's proposed ramp-up rate overleaf.

These issues of ramp-up and scaling are best addressed by the Auto-ID Community. An effort to create a practical road-map is currently underway. The key point is that a prototype chip does not automatically ensure the mass availability of chips; capacity constraints and price-elasticity issues will most certainly come into play, and delay wide-spread availability for at least several years. At this point, however, the Auto-ID Center remains focused on the goal of achieving the 5¢ RFID tag as a prototype independently of these commercial issues. Scaling, commercialization and pricing issues are best taken up by the vendor community.

Figure 8

ALIEN TECHNOLOGY'S PROPOSED RAMP-UP RATE



7. CONCLUSIONS

The researchers of the Auto-ID Center believe that the goal of the 5¢ tag is a difficult but achievable goal. The key conclusion is, that this goal cannot be achieved merely from the scaling up of existing silicon manufacturing processes to high volumes. The goal can only achieved by recognizing that RFID tags are different from conventional IC's. The Center and its sponsors have assembled a series of new technological approaches and have undertaken to produce a prototype 5¢ in the next 12 months.

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