CHAPTER XII

ADVANCED APPLICATIONS

12.1 SINUSOIDAL OSCILLATORS

One of the major hazards involved in the application of operational amplifiers is that the user often finds that they oscillate in connections he wishes were stable. An objective of this book is to provide guidance to help circumvent this common pitfall. There are, however, many applications that require a periodic waveform with a controlled frequency, waveshape, and amplitude, and operational amplifiers are frequently used to generate these signals.

If a sinusoidal output is required, the conditions that must be satisfied to generate this waveform can be determined from the linear feedback theory presented in earlier chapters.

12.1.1 The Wien-Bridge Oscillator

The Wien-bridge configuration (Fig. 12.1) is one way to implement a sinusoidal oscillator. The transfer function of the network that connects the output of the amplifier to its noninverting input is (in the absence of loading)

$$\frac{V_a(s)}{V_o(s)} = \frac{RCs}{R^2C^2s^2 + 3RCs + 1} \tag{12.1}$$

The operational amplifier is connected for a noninverting gain of 3. Combining this gain with Eqn. 12.1 yields for a loop transmission in this *positive*-feedback system

$$L(s) = \frac{3RCs}{R^2C^2s^2 + 3RCs + 1} \tag{12.2}$$

The characteristic equation

$$1 - L(s) = 1 - \frac{3RCs}{R^2C^2s^2 + 3RCs + 1} = \frac{R^2C^2s^2 + 1}{R^2C^2s^2 + 3RCs + 1} \tag{12.3}$$

has imaginary zeros at $s = \pm(j/RC)$, and thus the system can sustain constant-amplitude sinusoidal oscillations at a frequency $\omega = 1/RC$.

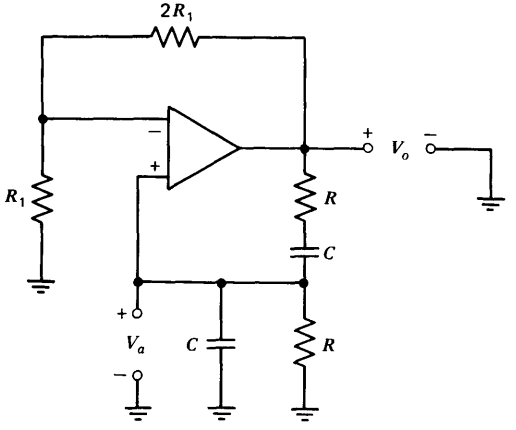


Figure 12.1 Wien-bridge oscillator.

12.1.2 Quadrature Oscillators

The quadrature oscillator (Fig. 12.2) combines an inverting and a non-inverting integrator to provide two sinusoids time phase shifted by 90° with respect to each other. The loop transmission for this connection is

$$L(s) = \left[-\frac{1}{R_1C_1s}\right]\left[\frac{R_3C_3s + 1}{(R_2C_2s + 1)R_3C_3s}\right] \tag{12.4}$$

In this expression, the first bracketed term is the closed-loop transfer function of the left-hand operational amplifier (the inverting integrator),

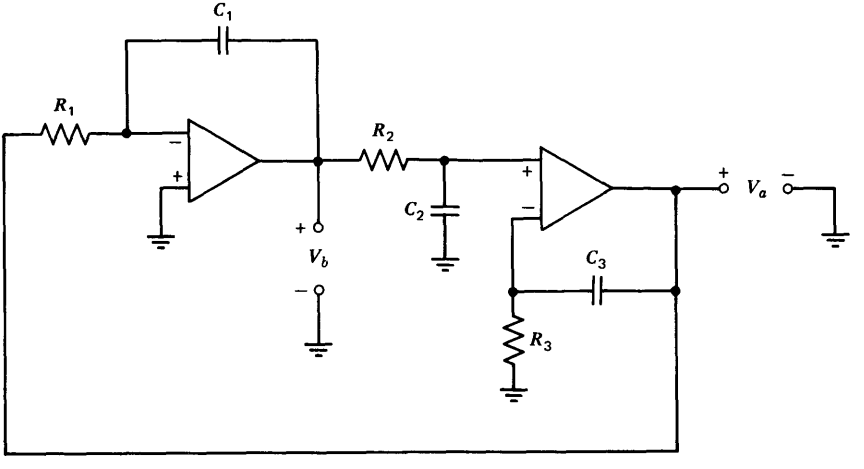


Figure 12.2 Quadrature oscillator.

while the second bracketed expression is the closed-loop transfer function of the right-hand operational amplifier. By proper selection of component values, the right-hand amplifier functions as a noninverting integrator. In fact, the discussion of this general connection in Section 11.4.1 shows that only the noninverting input of a differential connection is used as a signal input in this application.

If all three times constants are made equal so that $R_1C_1 = R_2C_2 = R_3C_3 = RC$, Eqn. 12.4 reduces to

$$L(s) = -\frac{1}{R^2C^2s^2} \tag{12.5}$$

The corresponding characteristic equation for this negative-feedback system is

$$1 - L(s) = 1 + \frac{1}{R^2C^2s^2} = \frac{R^2C^2s^2 + 1}{R^2C^2s^2} \tag{12.6}$$

Again, the imaginary zeros of Eqn. 12.6 indicate the potential for constant-amplitude sinusoidal oscillation. Note that, since there is an integration between V_a and V_b, these two signals will be phase shifted in time by 90° with respect to each other.

A similar type of oscillator (without an available quadrature output) can be constructed using a single amplifier configured as a double integrator (Fig. 11.12) with its output connected back to its input.

12.1.3 Amplitude Stabilization by Means of Limiting

There is a fundamental paradox that complicates the design of sinusoidal oscillators. A necessary and sufficient condition for the generation of constant-amplitude sinusoidal signals is that a pair of closed-loop poles of a feedback system lie on the imaginary axis and that no closed-loop poles are in the right half of the s plane. However, with this condition exactly satisfied (an impossibility in any but a purely mathematical system), the amplitude of the system output is determined by initial conditions. In any physical system, minor departure from ideal pole location results in an oscillation with an exponentially growing or decaying amplitude.

It is necessary to include some mechanism in the oscillator to stabilize its output amplitude at the desired level. One possibility is to design the oscillator so that its dominant pole pair lies slightly to the right of the imaginary axis for small signal levels, and then use a nonlinearity to limit amplitude to a controlled level. This approach was illustrated in Section 6.3.3 as an example of describing-function analysis and is reviewed briefly here.

Consider the Wien-bridge oscillator shown in Fig. 12.1. If the ratio of the resistors connecting the output of the amplifier to its inverting input is changed, it is possible to change the gain of the amplifier from 3 to $3(1 + \Delta)$. As a result, Eqn. 12.3 becomes

$$1 - L(s) = 1 - \frac{3(1 + \Delta)}{R^2C^2s^2 + 3RCs + 1} = \frac{R^2C^2s^2 - 3\Delta RCs + 1}{R^2C^2s^2 + 3RCs + 1} \quad (12.7)$$

The zeros of the characteristic equation (which are identically the closed-loop pole locations) become second order with $\omega_n = 1/RC$ and $\zeta = -(3/2)\Delta$. In practice, Δ is chosen to be large enough so that the closed-loop poles remain in the right-half plane for all anticipated parameter variations. For example, component-value tolerances or dielectric absorption associated with the capacitors alter the closed-loop pole locations.

Limiting can then be used to lower the value of Δ (in a describing-function sense) so that the output amplitude is controlled. Figure 12.3 shows one possible circuit where a value of $\Delta = 0.01$ is used. The oscillation frequency is 10^4 rad/sec or approximately 1.6 kHz. Output amplitude is (allowing for the diode forward voltage) approximately 20 V peak-to-peak. The symmetrical limiting is used since it does not add a d-c component or even harmonics to the output signal if the diodes are matched.

12.1.4 Amplitude Control by Parameter Variation

The use of a limiter to change a loop parameter in a describing-function sense after a signal amplitude has reached a specified value is one way to stabilize the output amplitude of an oscillator. This approach can result in significant harmonic distortion of the output signal, particularly when the oscillator is designed to function in spite of relatively large variations in element values. An alternative approach, which often results in significantly lower harmonic distortion, is to use an auxillary feedback loop to adjust some parameter value in such a way as to place the closed-loop poles precisely on the imaginary axis, precluding further changes in the amplitude of the oscillation, once the desired level has been reached. This technique is frequently referred to as automatic gain control, although in practice some quantity other than gain may be varied.

As an example of this type of amplitude stabilization, let us consider the effect on performance of varying resistor R_3 in the quadrature oscillator (Fig. 12.2). We assume that $C_1 = C_2 = C_3$, and that $R_1 = R_2 = R$, while $R_3 = (1 + \Delta)R$. In this case the loop transmission of the system (see Eqn. 12.4) is

$$L(s) = -\frac{(1 + \Delta)RCs + 1}{R^2C^2s^2(1 + \Delta)(RCs + 1)} \quad (12.8)$$

with a corresponding characteristic equation

$$1 - L(s) = \frac{R^3C^3(1 + \Delta)s^3 + R^2C^2(1 + \Delta)s^2 + RC(1 + \Delta)s + 1}{R^2C^2s^2(1 + \Delta)(RCs + 1)} \tag{12.9}$$

If we assume a small value for Δ, the zeros of the characteristic equation can be readily determined, since

$$R^3C^3(1 + \Delta)s^3 + R^2C^2(1 + \Delta)s^2 + RC(1 + \Delta)s + 1$$
$$\simeq \left[RC\left(1 + \frac{\Delta}{2}\right)s + 1\right]\left[R^2C^2\left(1 + \frac{\Delta}{2}\right)s^2 + RC\frac{\Delta}{2}s + 1\right]$$
$$|\Delta| \ll 1 \tag{12.10}$$

The performance of the oscillator is, of course, dominated by the complex-conjugate root pair indicated in Eqn. 12.10, and this pair has a natural frequency $\omega_n \simeq 1/RC$ and a damping ratio $\zeta \simeq \Delta/4$. The important feature is that the closed-loop poles can be made to lie in either the left half or the right half of the s plane according to the sign of Δ.

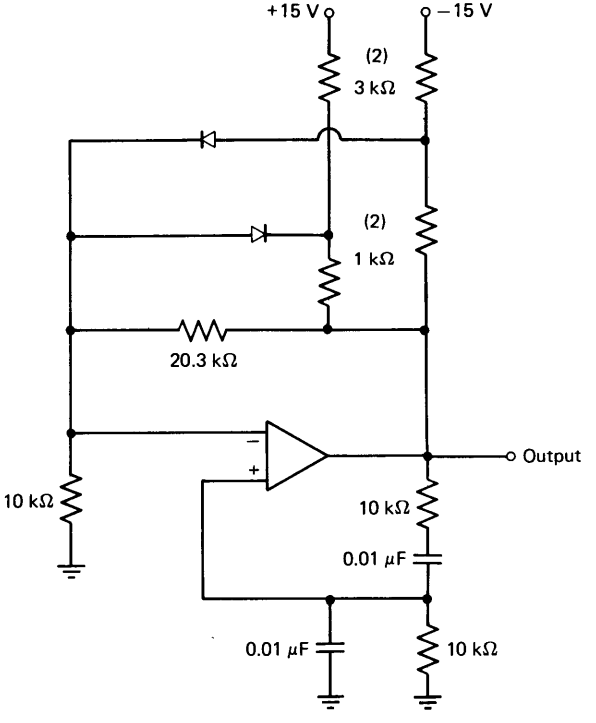


Figure 12.3 Wien-bridge oscillator with limiting.

The design of the amplitude-control loop for a quadrature oscillator provides an interesting and instructive example of the way that the feedback techniques developed in Chapters 2 to 6 can be applied to a moderately complex circuit, and for this reason we shall investigate the problem in some detail. The difficulties are concentrated primarily in the modeling phase of the analytical effort.

Our intent is to focus on amplitude control, and this control is to be accomplished by moving the closed-loop poles of the oscillator to the left- or the right-half plane according to whether the actual output amplitude is too large or too small, respectively. We assume that the signal $v_A(t)$ (see Fig. 12.2) has the form

$$v_A(t) = e_A(t) \sin \omega t \tag{12.11}$$

This representation, which models the signal as a constant-frequency sinusoid with a variable envelope $e_A(t)$, is not exact, because the instantaneous frequency of the sinusoidal component of v_A is a function of Δ. However, if the amplitude-control loop has a very low crossover frequency compared to the frequency of oscillation so that magnitude changes are relatively slow, we can consider the amplitude e_A alone and ignore the sinusoidal portion of the expression. In this case the exact frequency of the sinusoid is unimportant.

In order to find the dependence of v_A on the control parameter Δ, assume that the circuit is oscillating with $\Delta = 0$ so that the closed-loop poles of the oscillator are precisely on the imaginary axis. With this constraint the envelope is constant with some operating point value E_A so that

$$v_A(t) = E_A \sin \omega t \tag{12.12}$$

where $\omega = 1/RC$. If Δ undergoes an incremental step change to a new value Δ_1 at time $t = 0$, the oscillator poles move into the left-half plane (for positive Δ_1), and

$$v_A(t) \simeq E_A\, e^{-\zeta\omega_n t} \sin \omega_n t \tag{12.13}$$

Inserting values for ζ and ω_n from Eqn. 12.10 into Eqn. 12.13 yields

$$v_A(t) \simeq E_A\, e^{-(\Delta_1 t/4RC)} \sin \frac{t}{RC} \tag{12.14}$$

The envelope for this signal is

$$e_A(t) = E_A e^{-(\Delta_1 t/4RC)} = E_A \left[1 - \frac{\Delta_1 t}{4RC} + \frac{1}{2}\left(\frac{\Delta_1 t}{4RC}\right)^2 - \cdots + \right] \tag{12.15}$$

If $\Delta_1 t/4RC$ is small (a condition insured by a sufficiently small value of Δ_1), we can separate $e_A(t)$ into operating-point and incremental components as

$$e_A(t) = E_A + e_a(t) \simeq E_A - \frac{E_A \Delta_1}{4RC} t \tag{12.16}$$

Thus a positive incremental step change in Δ leads to an incremental envelope change that is a linearly decreasing function of time. This condition implies that the linearized transfer function that relates envelope amplitude to Δ is

$$\frac{E_a(s)}{\Delta(s)} = -\frac{E_A}{4RCs} \tag{12.17}$$

This linearized analysis confirms the feeling that control of the value of Δ is in fact a reasonable way to stabilize the amplitude of the oscillation, since the incremental change in the envelope of the oscillation is proportional to the time integral of Δ.

Further design of the amplitude-control loop depends on the actual topology of the system. Figure 12.4 shows one possible implementation in mixed circuit and functional block-diagram form. The envelope of the signal to be controlled is determined by an amplitude-measuring circuit. This circuit may be a simple diode-resistor-capacitor peak detector in cases where high precision is not required, or it may be an active "super-diode" type of connection (an example is given in Section 12.5.1) in more demanding applications. In either case, the design of this circuit is not particularly difficult and will not be discussed here. The envelope of the signal is compared with a reference value, and the resulting error signal passes through a linear controller with a transfer function $a(s)$. The output of the controller is used to drive a field-effect transistor that functions as a variable resistor whose value determines Δ.

The FET connection incorporates local compensation to linearize its characteristics as shown in the following development. If a junction FET is biased into conduction with a small voltage applied across its channel, and its gate reverse biased with respect to its channel, the drain current is approximately related to terminal voltages as

$$i_D = K\left[(v_{GS} + V_P)v_{DS} - \frac{v_{DS}^2}{2}\right] \tag{12.18}$$

where K is a constant dependent on transistor construction, and V_P is the magnitude of the gate-to-source pinch-off voltage.

The dependence of i_D on the square of the drain-to-source voltage is undesirable, since this term represents a nonlinearity in the channel resist-

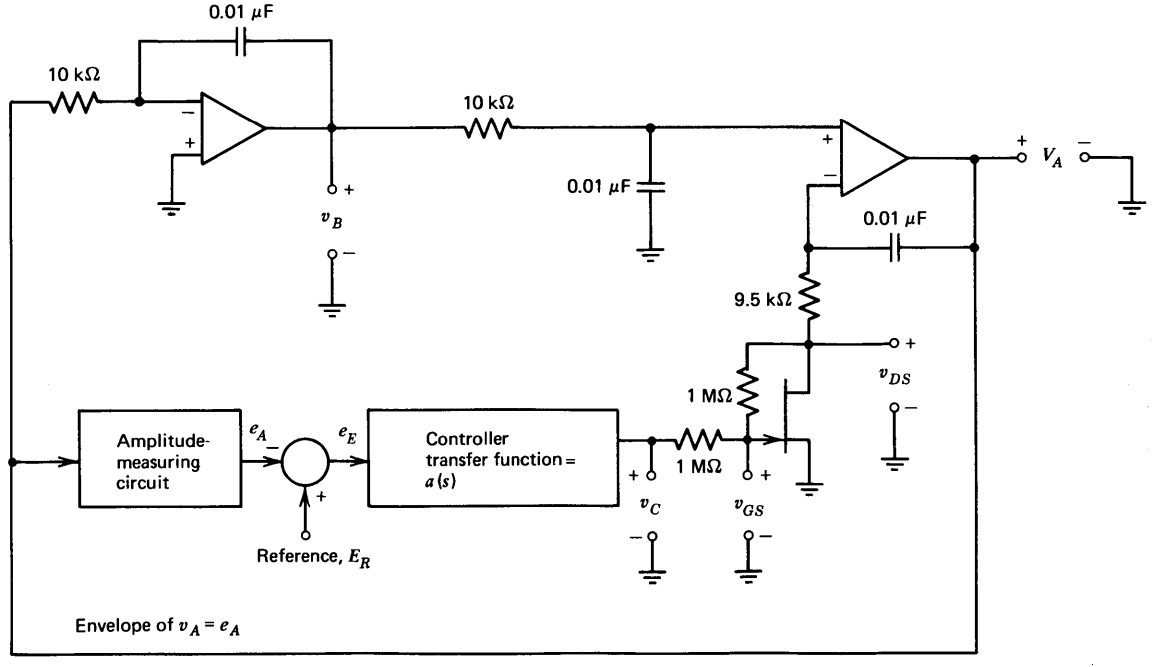


Figure 12.4 Quadrature oscillator with amplitude stabilization.

ance of the device, and this nonlinearity will introduce harmonic distortion into the oscillator output. The nonlinearity can be eliminated by adding half of the drain-to-source voltage to the gate-to-source voltage via resistors as shown in Fig. 12.4. The resistors are large enough so that they do not significantly shunt the drain-to-source resistance of the FET under normal operating conditions. With the topology shown,

$$v_{GS} = \tfrac{1}{2}(v_C + v_{DS}) \tag{12.19}$$

Substituting Eqn. 12.19 into Eqn. 12.18 shows that

$$i_D = K\left[\left(\frac{v_C}{2} + \frac{v_{DS}}{2} + V_P\right)v_{DS} - \frac{v_{DS}^2}{2}\right] = K\left(\frac{v_C}{2} + V_P\right)v_{DS} \tag{12.20}$$

or

$$R_{DS} = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{K[(v_C/2) + V_P]} \tag{12.21}$$

This equation indicates that the incremental resistance of the FET is independent of drain-to-source voltage when the network is included.

For purposes of design, we assume that the FET is characterized by $V_P = 4$ volts and $K = 10^{-3}$ mho per volt. Recall that stable-amplitude oscillations require that all three R-C time constants be identical; thus the operating point value of R_{DS} is 500 ohms. Equation 12.21 combined with FET parameters indicates that this value results with an operating-point value for the control voltage of -4 volts. The incremental change in R_{DS} as a function of the control voltage at this operating point, obtained by differentiating Eqn. 12.21 with respect to v_C,

$$\left.\frac{\partial R_{DS}}{\partial v_C}\right|_{v_C = -4\text{ V}} = -125\ \Omega/\text{V} \tag{12.22}$$

Earlier modeling was done in terms of Δ, the fractional deviation of the resistance R_3 in Fig. 12.2 from its nominal value. This resistor consists of the FET plus a 9.5 kΩ resistor in the actual implementation. The incremental dependence of Δ on the control voltage is determined by dividing Eqn. 12.22 by the anticipated operating-point value of the total resistance, 10 kΩ. Thus

$$\left.\frac{\partial \Delta}{\partial v_C}\right|_{v_C = -4\text{ V}} = -0.0125\ \text{V}^{-1} \tag{12.23}$$

The relationships summarized in Eqns. 12.17 and 12.23 combined with the system topology and an assumed operating-point value for the envelope $E_A = 10$ volts lead to the linearized block diagram for the amplitude-

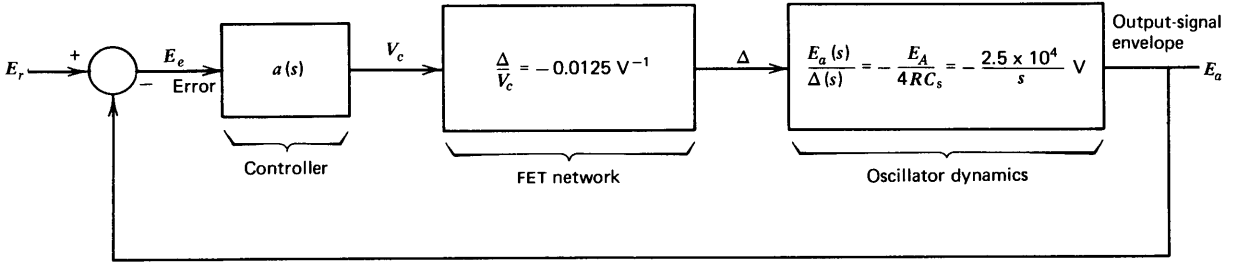


Figure 12.5 Linearized block diagram for amplitude-control loop.

control loop shown in Fig. 12.5. The negative of the loop transmission for this system is

$$\frac{E_a(s)}{E_e(s)} = a(s) \times \frac{312.5}{s} \tag{12.24}$$

A number of factors govern the choice of $a(s)$ for this application including:

(a) The actual FET gate-to-source voltage required under quiescent conditions is strongly dependent on FET parameters and the exact values of the other components used in the circuit. The easiest way to insure that the difference between the envelope and the reference is constant in spite of these variable parameters is to include an integration in $a(s)$ since this integration forces the operating-point value of the error to zero.

(b) The analysis is predicated on a much lower crossover frequency for the amplitude-control loop than the frequency of oscillation, 10^4 radians per second. However, a very low frequency control loop accentuates the effect on amplitude of rapid changes in quantities like the supply voltages. A somewhat arbitrary compromise is to choose a crossover frequency of 100 radians per second.

(c) Since the analysis is based on a hierarchy of approximations, the system should be designed to have a very conservative phase margin.

(d) The controller transfer function should include low-pass filtering. The detector signal that indicates the envelope amplitude invariably includes components at the oscillation frequency or its harmonics. If these components are not filtered so that they are at an insignificant level when applied to the FET gate, the resultant channel-resistance modulation introduces distortion into the oscillator output signal.

A controller transfer function that incorporates these features is

$$a(s) = \frac{3.2(0.1s + 1)}{s(10^{-3}s + 1)^2} \tag{12.25}$$

The negative of the loop transmission with this value for $a(s)$ is

$$\frac{E_a(s)}{E_e(s)} = \frac{10^3(0.1s + 1)}{s^2(10^{-3}s + 1)^2} \tag{12.26}$$

The system crossover frequency is 100 radians per second, and phase margin exceeds 70° with this value for $a(s)$.

A possible circuit that provides the negative of the desired $a(s)$ is shown in Fig. 12.6. In many cases of practical interest, this inversion can be cancelled by some rearrangement of the amplitude-measuring circuit. The second required filter pole is obtained with a passive network. The filter

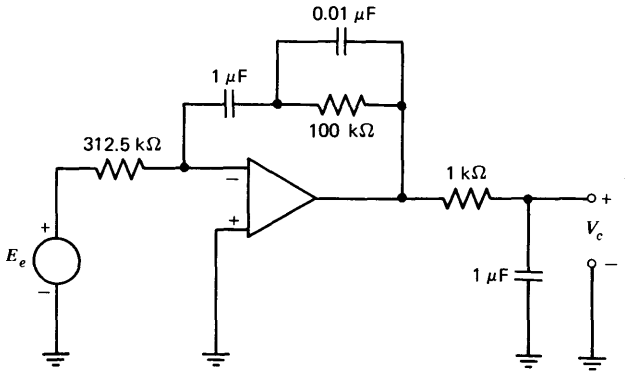


Figure 12.6 Controller circuit.

network impedance level is low enough so that the network is not disturbed by the 2-MΩ load connected to it.

The reference level required to establish oscillator amplitude can be applied to the controller by adding another input resistor to the operational amplifier. It may also be possible to realize part of the amplitude-measuring circuitry with this amplifier. An example of this type of function combination is given in Section 12.5.1.

Two practical considerations involved in the design of this oscillator deserve special mention. First, the signal v_B normally has lower harmonic distortion than does v_A since the integration of the first amplifier filters any harmonics that may be introduced by the FET. Second, it is possible to vary the reference amplitude for this circuit and thus modulate the amplitude of the oscillator output. However, the control bandwidth in this mode will be relatively small, and performance will change as a function of quiescent envelope amplitude since the loop-transmission magnitude is dependent on operating levels.

The performance of an oscillator of this type can be quite impressive. Amplitude control to within 1 mV peak-to-peak is possible if "superdiodes" are used in the envelope detector. Harmonic distortion of the output signal can be kept a factor of 10^4 or more below the fundamental component.

12.2 NONLINEAR OSCILLATORS

The discussion of oscillators up to this point has focused on the design of circuits that provide sinusoidal output signals. The basic approach is to use a linear, second-order feedback loop to generate the sinusoid, and then incorporate some mechanism to control amplitude.

Operational amplifiers are also frequently used in nonlinear oscillator circuits that intentionally produce nonsinusoidal output signals. The analysis of these types of oscillators is complicated by the fact that transform methods normally cannot be used. One frequently used technique for evaluating the performance of these types of oscillators is to determine the output and internal signals directly via time-domain calculations.

12.2.1 A Square- and Triangle-Wave Generator

A function generator that produces square and triangle waves as its outputs was used as an example of describing-function analysis in Section 6.3.3. This topology combines an integrator with a Schmitt-trigger circuit. The Schmitt trigger can be realized by applying *positive* feedback around an operational amplifier, as shown in Fig. 12.7.[1] Consider operation with v_I a large positive voltage. In this case the amplifier will be saturated with a positive output voltage.

It is assumed that the output-voltage magnitude is limited to a maximum value of V_M. This limiting can be accomplished in several ways. If relatively crude level control is sufficient, the saturation levels may be determined simply by power-supply voltages and internal amplifier voltage drops. Somewhat better control is possible if an amplifier such as the LM101A (see Section 10.4.1) is used. The output level of this circuit can be limited by connecting diode clamps to a compensation terminal. A third possibility is to follow the operational amplifier shown with a precision limiter similar to those described in Section 11.5.3, and to apply positive feedback around the entire connection. This approach has the further advantage that the output element is operating with local negative feedback and thus has very low output resistance.

In order to force the circuit to change state, the input voltage is lowered. When the input level reaches approximately $-(R_1/R_2)V_M$, the noninverting input of the amplifier is close to ground potential and the device enters its linear operating region. The massive positive feedback that results with the amplifier active sweeps its output negative until a level of $-V_M$ is reached. Further negative changes in input voltage do not affect the output. If the input voltage is raised, the amplifier enters its active region at an

[1] In many practical circuits, a comparator rather than an operational amplifier is used to implement a Schmitt trigger. A comparator, like an operational amplifier, is a high-gain, direct-coupled amplifier. However, since it is not intended for use in negative-feedback connections, the frequency-response compromises that must be made to insure the stability of an operational amplifier need not be included in the comparator design. Consequently, the response time of a Schmitt trigger realized via a comparator can be significantly faster than that obtained using an operational amplifier.

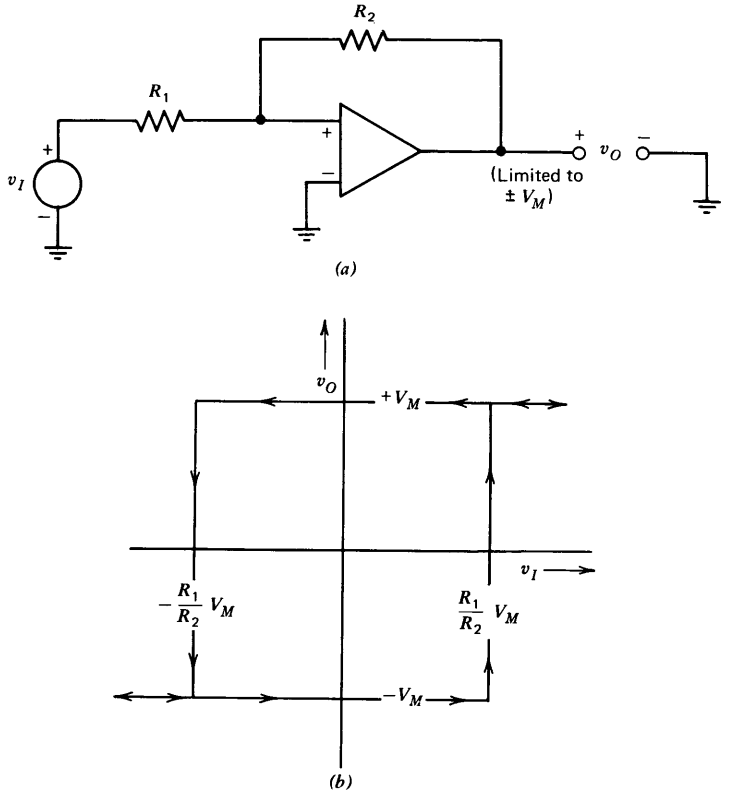


Figure 12.7 Schmitt trigger. (*a*) Circuit. (*b*) Characteristics.

input level of $+(R_1/R_2)V_M$, and is then driven to positive saturation. These transition points combine to give the characteristics shown in Fig. 12.7*b*.

A possible oscillator connection using this type of Schmitt trigger is shown in Fig. 12.8. With the modulating voltage $v_C = 0$, signal waveforms are as shown in part *b* of this figure. The period of oscillation is determined by noting that the magnitude of the slope of the triangle wave is always $10/RC$, and that the total change in the voltate level of v_A is 40 volts for one complete cycle. Therefore

$$\tau = \frac{40}{10/RC} = 4RC \tag{12.27}$$

The corresponding frequency of oscillation is

$$f = \frac{1}{\tau} = \frac{1}{4RC} \tag{12.28}$$

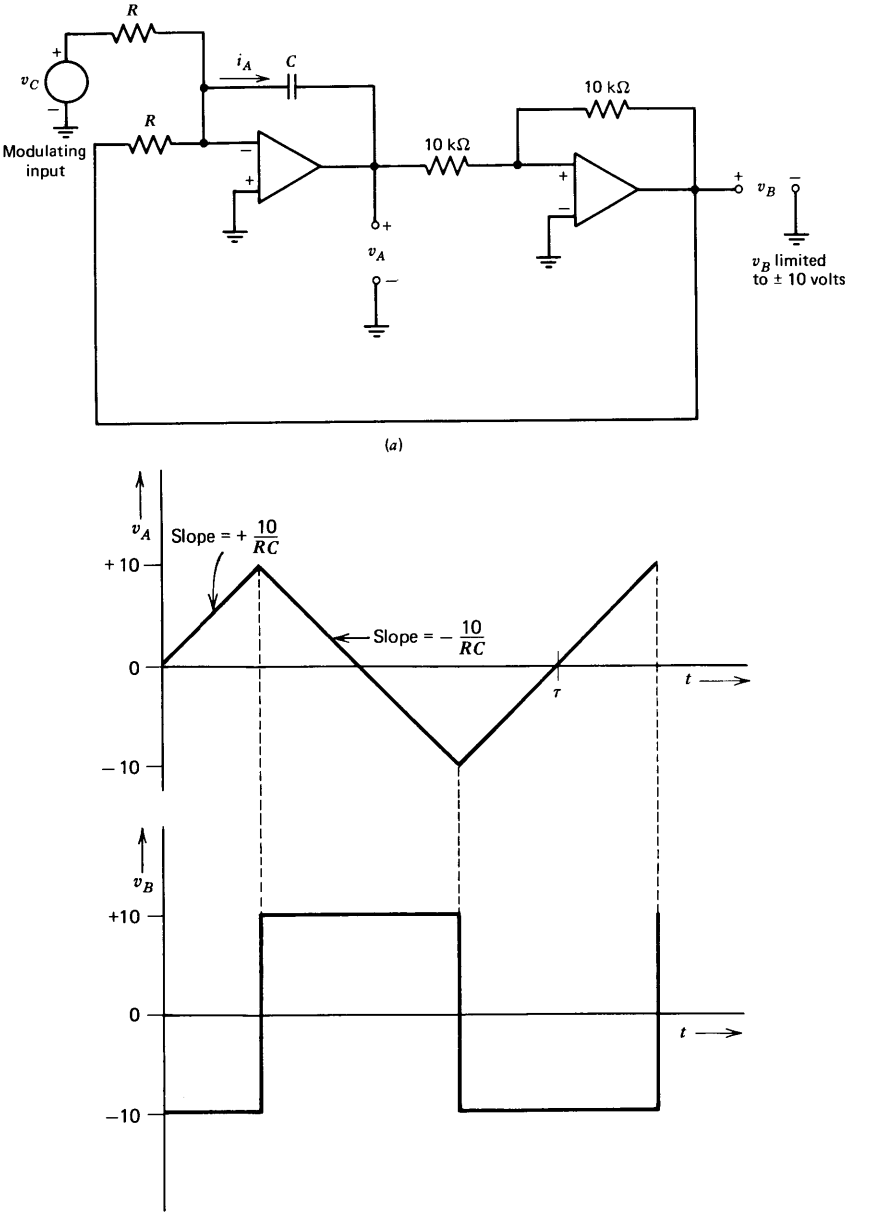
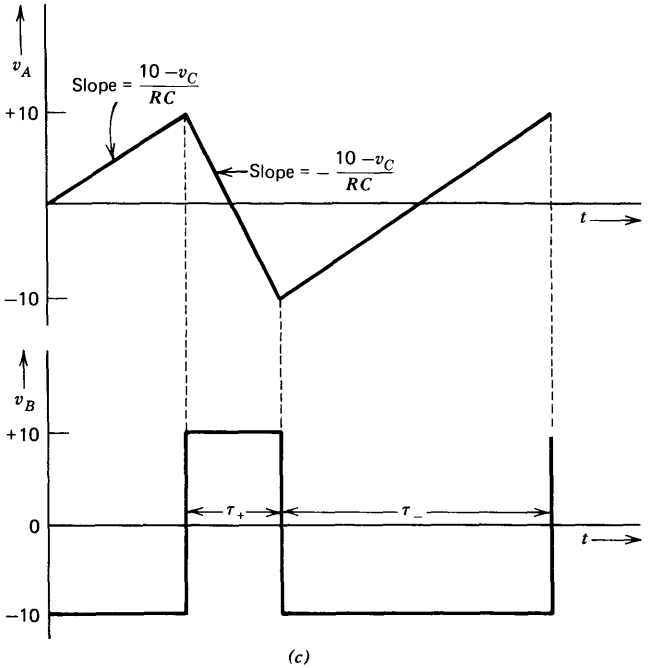


Figure 12.8 Nonlinear oscillator. (*a*) Circuit. (*b*) Waveforms with $v_C = 0$. (*c*) Waveforms with $|v_C| < 10$ volts.



(c)

Figure 12.8—Continued

In commercial versions of this circuit, decade frequency switching is frequently accomplished by changing capacitors, while variation of the value of resistor R provides vernier control in any one decade.

12.2.2 Duty-Cycle Modulation

The current that charges the capacitor can be modulated by means of an applied voltage v_C, with this current given by

$$i_A = \frac{v_C + v_B}{R} \tag{12.29}$$

A positive value for v_C increases capacitor charging current when v_B is positive and decreases this current when v_B is negative. The net result is to duty-cycle modulate the signal v_B as shown in Fig. 12.8c. The fraction of the time this signal stays positive is

$$\frac{\tau_+}{\tau_+ + \tau_-} = \frac{20RC/(10 + v_C)}{20RC/(10 + v_C) + 20RC/(10 - v_C)} = \frac{1}{2}\left(1 - \frac{v_C}{10}\right) \tag{12.30}$$

This duty-cycle modulator has a number of interesting features that make it useful in a variety of applications. Equation 12.30 shows that the duty cycle is linearly proportional to v_C and changes from one to zero as v_C changes from -10 volts to $+10$ volts. However, maximum capacitor charging current is limited to twice its value with zero v_C, so that the time spent in the shorter of the two periods is never less than half its quiescent value. The frequency of operation is a nonlinear function of v_C and is given by

$$f = \frac{1}{\tau_+ + \tau_-} = \frac{1}{20RC/(10 + v_C) + 20RC/(10 - v_C)} = \frac{100 - v_C^2}{400RC} \quad (12.31)$$

This equation shows that the frequency is lowered by any nonzero value of v_C.

Applications include the control of switching power amplifiers and the realization of the type of analog multiplier shown in Fig. 12.9. In this circuit, the duty-cycle modulator controls the state of a switch that is frequently realized with field-effect transistors. The circuit is arranged so that the switch arm is connected to a voltage $+v_Y$ for a fraction of the time $\frac{1}{2}[1 + (v_X/V_R)]$, and to a voltage $-v_Y$ for the remainder of the time, a fraction equal to $\frac{1}{2}[1 - (v_X/V_R)]$. (Alternative implementations use current rather than voltage switching to increase switching speed.) The output filter (usually a multiple-order active filter rather than the simple network shown) averages the switch voltage v_S, so that

$$v_O = \overline{v_S} = +v_Y\left[\frac{1}{2}\left(1 + \frac{v_X}{V_R}\right)\right] - v_Y\left[\frac{1}{2}\left(1 - \frac{v_X}{V_R}\right)\right] = \frac{v_X v_Y}{V_R} \quad (12.32)$$

where the over bar indicates time averaging. Note that the voltage V_R (which is equal to the maximum magnitude of the signal out of the Schmitt

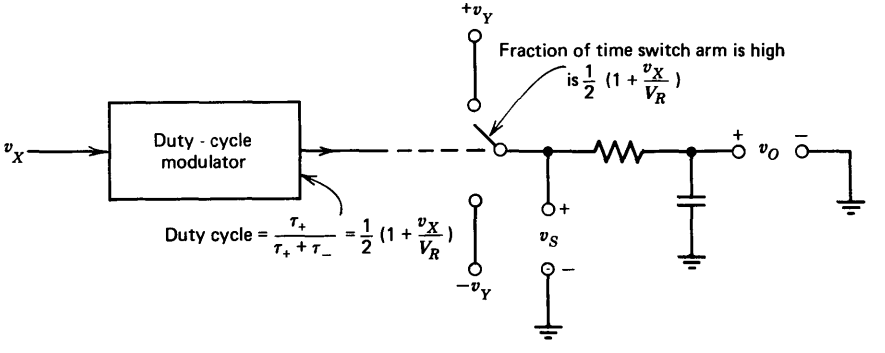


Figure 12.9 Time-division multiplier.

trigger) can be varied to mechanize division. A technique for varying the signal from the Schmitt trigger is described below.

Versions of this type of multiplier that limit errors to 0.05% of maximum output have been designed.

12.2.3 Frequency Modulation

Another variation of the basic nonlinear oscillator shown in Fig. 12.10 results in an oscillator with a voltage-controlled operating frequency. Here the Schmitt trigger determines the state of a switch that allows a variable-level voltage to be applied to the integrator. If the Schmitt trigger switches at input-signal levels of $\pm V_T$ the total excursion of the signal v_A will be $4\ V_T$ volts per cycle. The slope of signal v_A has a magnitude of v_F/RC volts per second, and thus the frequency of oscillation is

$$f = \frac{v_F/RC}{4V_T} = \frac{v_F}{4V_TRC} \tag{12.33}$$

12.2.4 A Single-Amplifier Nonlinear Oscillator

The operational amplifier used as an integrator in the nonlinear oscillator described above can be replaced with a passive resistor-capacitor network a shown in Fig. 12.11, resulting in a configuration first reported by Bose.[2] The Schmitt trigger functions in an inverting mode in this connection so that a sufficiently positive level for v_A saturates the amplifier output at $-V_M$. Switching points occur at $v_A = \pm V_M R_1/(R_1 + R_2)$. If the dotted modulating resistor is omitted, the waveforms are as shown in Fig. 12.11*c*. The capacitor voltage is a sequence of exponential segments rather than a true triangular wave. The duty cycle of the signal can be modulated by including the dotted resistor shown in Fig. 12.11*a*. If the width of the hysterisis region is made very small by choosing $R_1 \ll R_2$, the current into the capacitor becomes nearly constant in each state, since the circuit keeps the capacitor voltage close to zero. In this case, the duty cycle of the voltage v_O is linearly related to control voltage v_C.

12.3 ANALOG COMPUTATION

It was mentioned in Chapter 1 that operational amplifiers were initially used primarily for analog computation. The objective in analog computation is to build an electrical network, using operational amplifiers and

[2] A. G. Bose, "A Two-State Modulation System," 1963 Wescon Convention Record, Part 6, Paper 7.1.

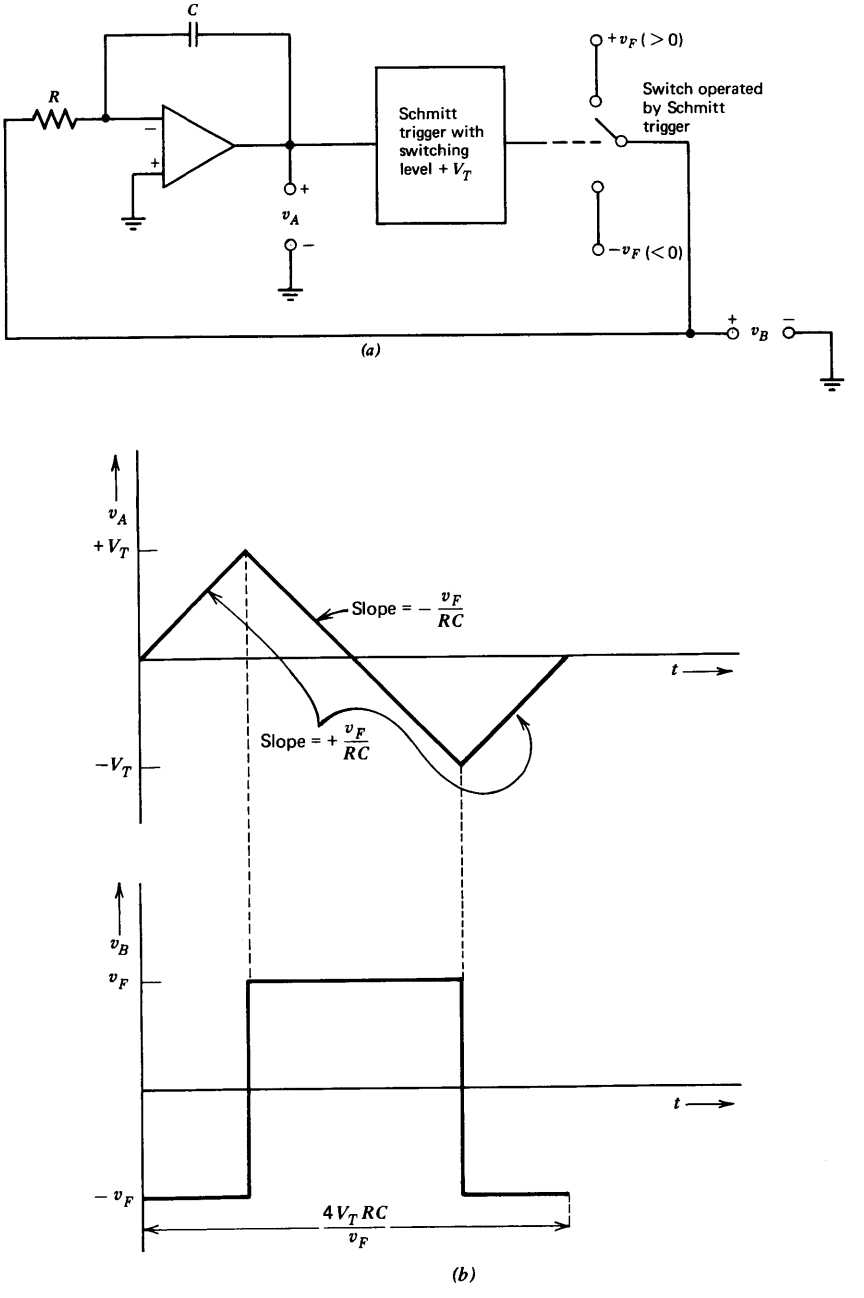


Figure 12.10 Voltage-controlled oscillator. (*a*) Circuit. (*b*) Waveforms.

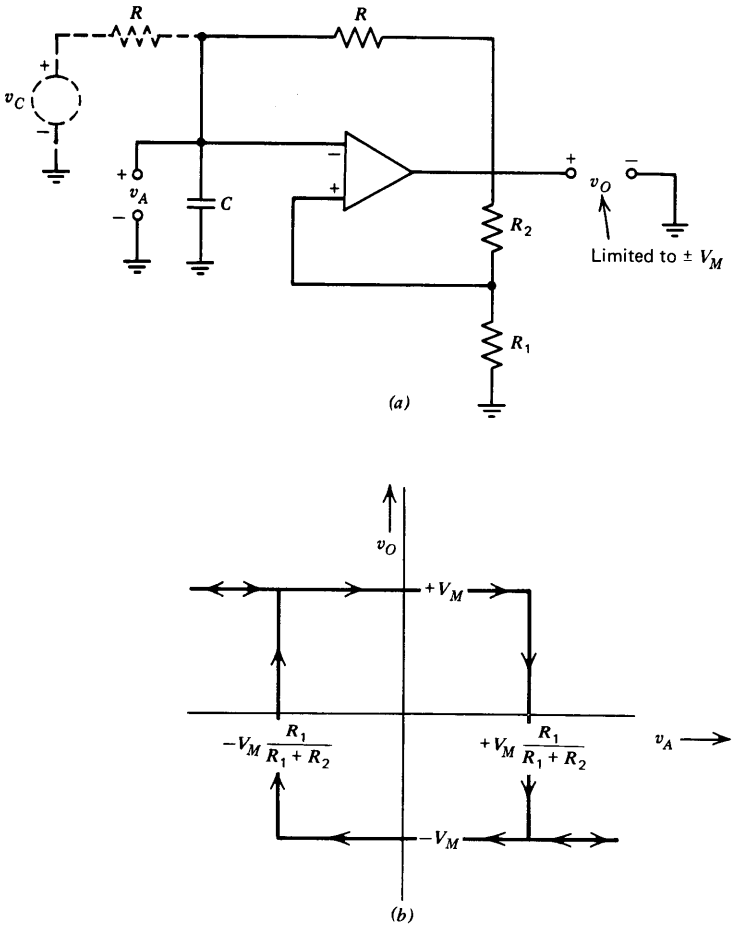


Figure 12.11 One amplifier nonlinear oscillator. (*a*) Circuit. (*b*) Inverting Schmitt-trigger characteristics. (*c*) Waveforms.

associated components, that obeys the same differential equation as does the system under study. The answers obtained consist of the responses of the electrical analog to particular inputs and initial conditions.

Analog computers are available from several manufacturers. These machines incorporate, in addition to the necessary hardware, a considerable human-engineering effort. Summing amplifiers and integrators included in these machines are normally constructed with fixed scale factors so that external components need not be used. For example, several inputs with gains of -1 and -10 are typically provided for each summing amplifier.

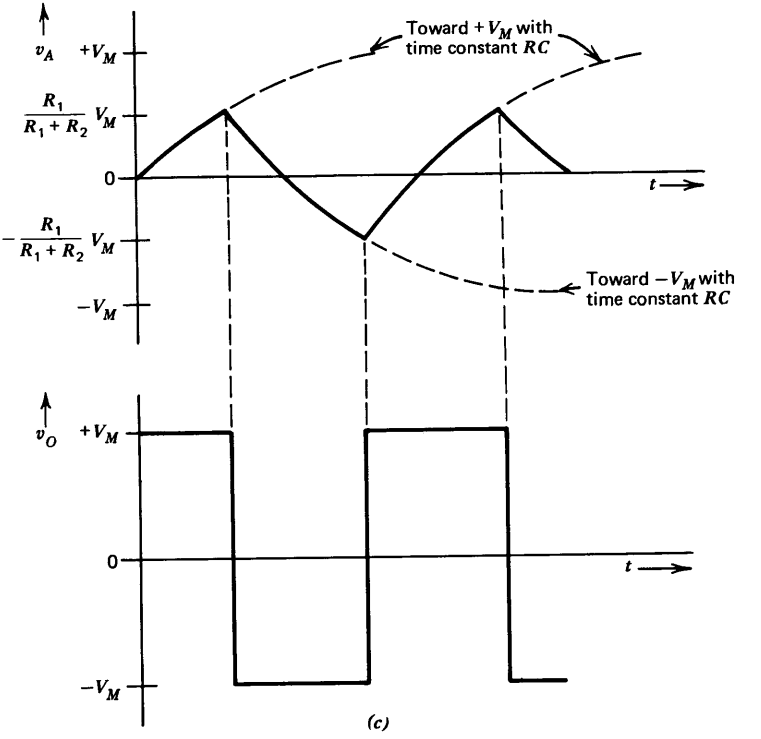


Figure 12.11—Continued

Potentiometers are also included, and these devices are combined with fixed-gain amplifiers to provide arbitrary gain levels. Thus a gain of -3.12 might be realized by preceding a gain of -10 amplifier with a potentiometer set for an attenuation of 0.312. Nonlinear elements such as function generators and multipliers are frequently included. The inputs and outputs of the various elements are usually connected to jacks of some type. The interconnections necessary to simulate a particular system are then made with patchcords that connect the various jacks. In many cases, the programming (inserting the patchcords to establish the proper connection pattern) is done on a board physically removed from the computer while other users, with their own boards, solve their problems. The board makes the required connections when it is inserted into a mating plate located on the machine.

While the accuracy of solutions obtained via analog computation is limited by component tolerances, it normally far exceeds the accuracy required for the simulation of physical systems, which are themselves constructed with imprecise components. A further consideration is that it is frequently

possible to get a good physical feeling for a system via analog computation, since many variables are available for observation, and since the effects of parameter variations can be quickly investigated.

Our treatment here can only cover the barest essentials and highlight a few of the ancillary circuits that were evolved for analog computation. The reader interested in a detailed treatment of this fascinating and powerful technique is referred to Korn and Korn.[3]

12.3.1 The Approach

Our objective here is to show how electronic-analog techniques are used to simulate differential equations that describe the systems to be studied. We initially assume that the differential equation under investigation is linear and has the general form

$$a_n \frac{d^n x}{dt^n} + a_{n-1} \frac{d^{n-1} x}{dt^{n-1}} + \cdots + a_1 \frac{dx}{dt} + a_0 x = f(t) \qquad (12.34)$$

It is certainly not necessary that the independent variable of the system under study be time as implied by Eqn. 12.34. For example, if we were investigating the deflection of a bridge under static load, we might be interested in vertical displacements from equilibrium as a function of distance from one end of the bridge. However, since our analog will use time as its independent variable, we substitute time for the independent variable if necessary in the original equation. Similarly, we realize that any dependent variables in our analog will have to be voltages, regardless of the variables they actually represent in the system under study.

Equation 12.34 is rewritten so that the highest derivative of x is expressed in terms of the other variables in the form

$$\frac{d^n x}{dt^n} = -\frac{a_{n-1}}{a_n} \frac{d^{n-1} x}{dt^{n-1}} - \cdots - \frac{a_1}{a_n} \frac{dx}{dt} - \frac{a_0 x}{a_n} + \frac{1}{a_n} f(t) \qquad (12.35)$$

Equation 12.35 can be represented as the block diagram shown in Fig. 12.12. In this representation, the variable $d^n x/dt^n$ appears as the output of a summation point. Inputs to the summation point are scaled multiples of the driving function and the lower-order derivatives of x. The lower-order derivatives are obtained by successive integrations of $d^n x/dt^n$, with a total of n integrations required to complete the block diagram.

Note that the only elements included in the block diagram are a multiple-input summation point, inverters to precede some inputs on the summer,

[3] G. A. Korn and T. M. Korn, *Electronic Analog and Hybrid Computers*, 2nd Edition, McGraw-Hill, New York, 1972.

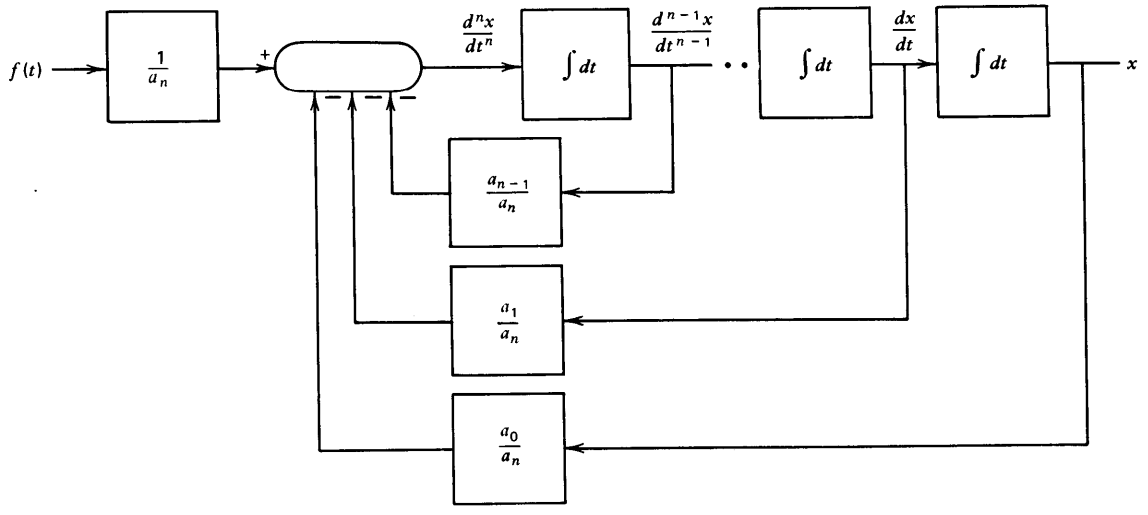


Figure 12.12 Block diagram of Eqn. 12.35.

gain blocks, and integrators. Since each of these elements can be readily constructed using operational amplifiers and passive components, the block diagram can be implemented using these devices. When the analog realization is excited with a voltage equal to $f(t)$, voltages equal in value to x and its derivatives will be available as the outputs of the integrators.

As an example of this process, consider the differential equation

$$\frac{d^4x}{dt^4} + 2.61\frac{d^3x}{dt^3} + 3.42\frac{d^2x}{dt^2} + 2.61\frac{dx}{dt} + x = f(t) \qquad (12.36)$$

(We recall from Section 3.3.2 that this equation represents a fourth-order Butterworth filter.) Solving for d^4x/dt^4 yields

$$\frac{d^4x}{dt^4} = -2.61\frac{d^3x}{dt^3} - 3.42\frac{d^2x}{dt^2} - 2.61\frac{dx}{dt} - x + f(t) \qquad (12.37)$$

One possible simulation of this equation is shown in Fig. 12.13. The voltages expected at the output of various amplifiers are indicated by writing the value of the variable the voltage represents at appropriate nodes. Note that in contrast to traditional analog-computer methods, gains are established by selecting impedances[4] used around operational amplifiers rather than by combining potentiometers with fixed-gain amplifiers and integrators. Also, functions have been combined in order to reduce the number of amplifiers required. The use of inverting connections only is traditional in analog computation, and reflects that fact that an operational-amplifier design technique frequently used to improve d-c performance results in an amplifier that can only be used in inverting connections. (See Section 12.3.3.) It may, of course, be possible to use noninverting integrators or summing amplifiers (realized with resistive summing at the input to a noninverting-amplifier connection) if general-purpose operational amplifiers are used for this simulation.

The four integrators appear along the top of the diagram. Since it is assumed that there is no need to have a voltage representing d^4x/dt^4 available, the summing operation is included in the first integrator connection. The output of this integrator is $-(d^3x/dt^3)$ when the indicated current is equal to $(10^{-6}$ A) d^4x/dt^4. Since inverting integrators are used, the signs associated with successive derivatives alternate. The scaling and inversions required by the coefficients of x and its second derivative are obtained with the bottom amplifier.

[4] The relative impedance levels shown in Fig. 12.13 are high if general-purpose operational amplifiers such as the LM101A are used. Since only ratios are important in establishing the transfer function, all impedance levels can be scaled to reduce errors that result from amplifier input currents.

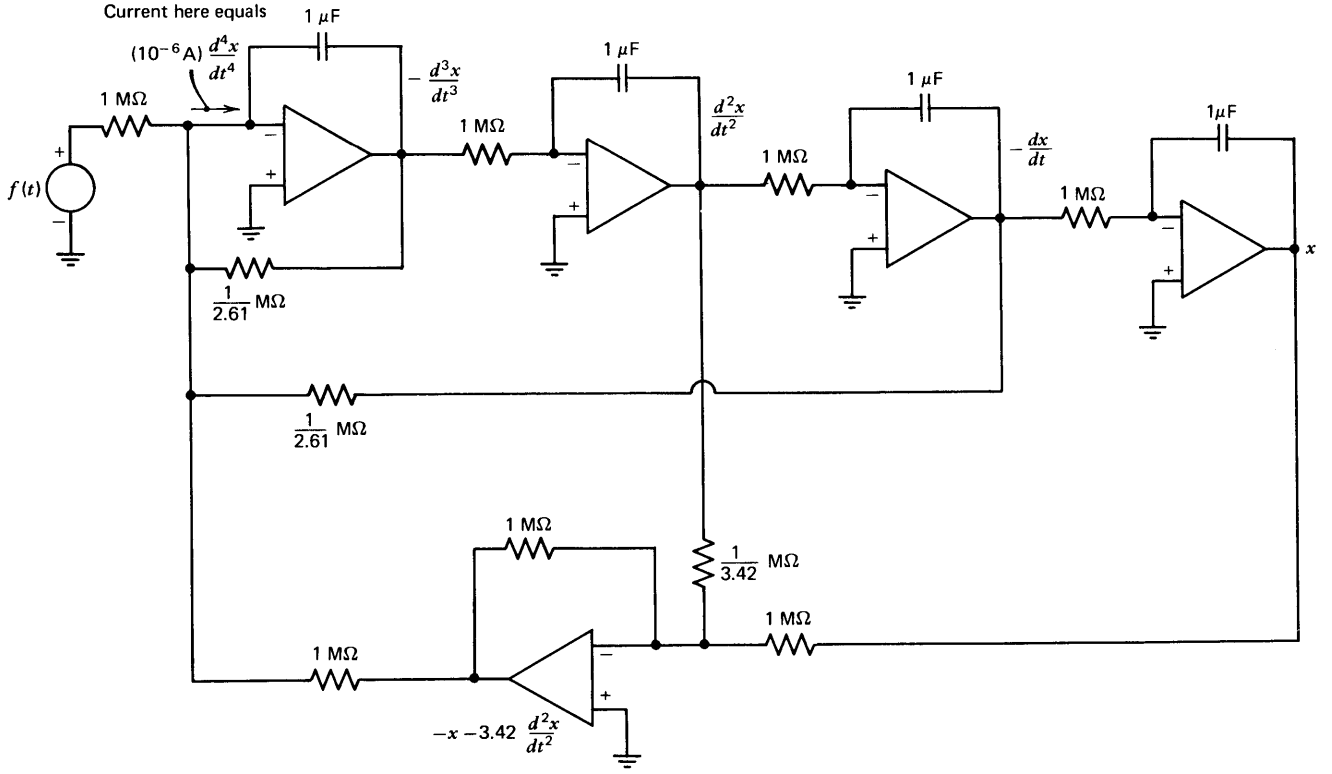


Figure 12.13 Simulation of fourth-order Butterworth equation.

The number of amplifiers required in Fig. 12.13 indicates the general rule. If this topology is used, simulating an nth-order linear differential equation requires n integrators and one amplifier that inverts appropriate signals as necessary to complete feedback paths.

Analog-computing techniques can also be used to solve a variety of nonlinear differential equations by including hardware that implements the nonlinearity in the simulation. As an example, consider Van der Pol's differential equation

$$\frac{d^2x}{dt^2} + \mu(x^2 - 1)\frac{dx}{dt} + x = 0 \tag{12.38}$$

where μ is a positive constant.

For small values of x, the coefficient of the first derivative term is negative, and increasing-amplitude oscillations result. When the amplitude of the oscillation becomes large enough, the coefficient of the first derivative will be positive over part of the cycle, and a limit cycle can result. Equation 12.38 is rewritten in a form convenient for simulation as

$$\frac{d^2x}{dt^2} = -\mu x^2 \frac{dx}{dt} + \mu \frac{dx}{dt} - x \tag{12.39}$$

Multipliers are required to generate x^2 and form the $x^2(dx/dt)$ product necessary for the simulation of Eqn. 12.39. Two techniques for analog multiplication were described in Sections 11.5.5 and 12.2.2. Practical multipliers based on these methods are often designed to have an output voltage equal to the product of the two input voltages divided by 10 volts for compatibility with the dynamic range of most solid-state operational amplifiers. Figure 12.14 shows a possible simulation of Eqn. 12.39 assuming that multipliers with this scale factor are used.

Van der Pol's equation is an example of an undriven differential equation, and excitation is by initial conditions only. While initial conditions were not mentioned in our earlier discussion of the simulation of linear differential equations, we recognize that we must specify n initial conditions in order to determine the complete (homogeneous plus driven) solution of an nth-order differential equation. These initial conditions can be set simply by establishing the voltages on the integrating capacitors at time $t = 0$, since these voltages are proportional to the values of x and its first $n - 1$ derivatives. A circuit for setting initial conditions is described in Section 12.3.3.

The value of x as a function of time for Van der Pol's equation with $\mu = 0.25$ is shown in Fig. 12.15. The initial conditions used for parts a and b of this figure are $x(0) = 0.5$, $(dx/dt)(0) = 0$ and $x(0) = 3$, $(dx/dt)(0) = 0$, respectively. We see that in both cases the amplitude of the limit cycle con-

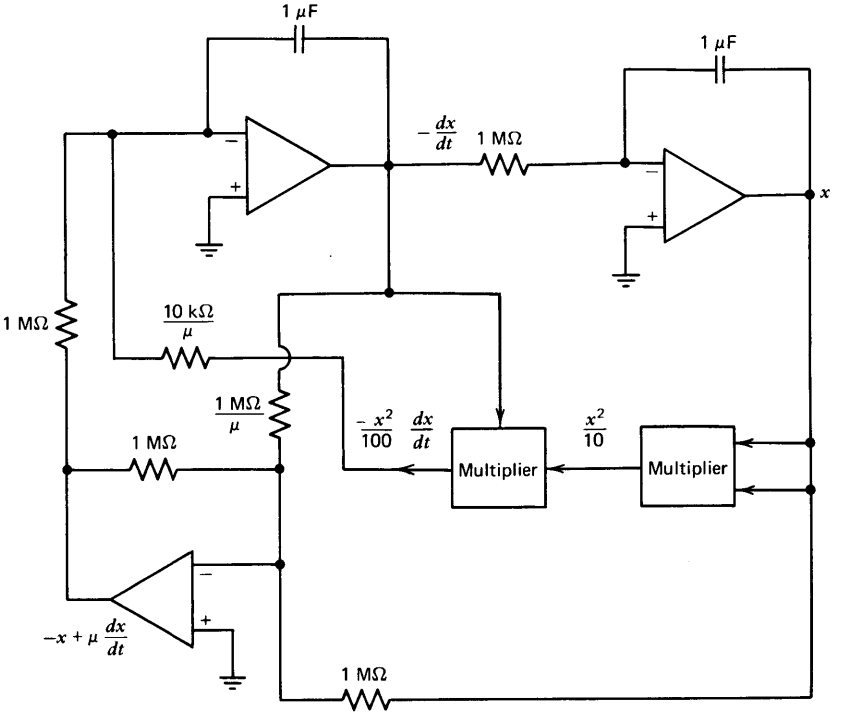


Figure 12.14 Simulation of Van der Pol's equation.

verges to a peak-to-peak value of approximately 4. Part *c* of this figure is a plot of dx/dt versus $x(t)$. This representation, in which time is a parameter along the curve, is called a *phase-plane* plot. The responses for both values of initial conditions are included. The convergence to equal-amplitude limit-cycles for both sets of initial conditions is evident in this figure.

The formal procedure described here is certainly not the only one which results in a correct analog representation of a problem. While it does lead to a compact realization, other realizations may maintain better correspondence with the physical system that is being modeled. One popular alternative technique involves simply drawing a block diagram for the system under study, and then implementing the block diagram on a block-by-block basis without ever writing down the complete system differential equation. While this approach often requires more hardware to complete the simulation, it is convenient in that voltages proportional to the actual variables of interest in the problem under study are avaliable. Furthermore, it is generally possible using this alternative to associate scale factors with the parameters of physical elements in the simulated systems on a one-to-one basis.

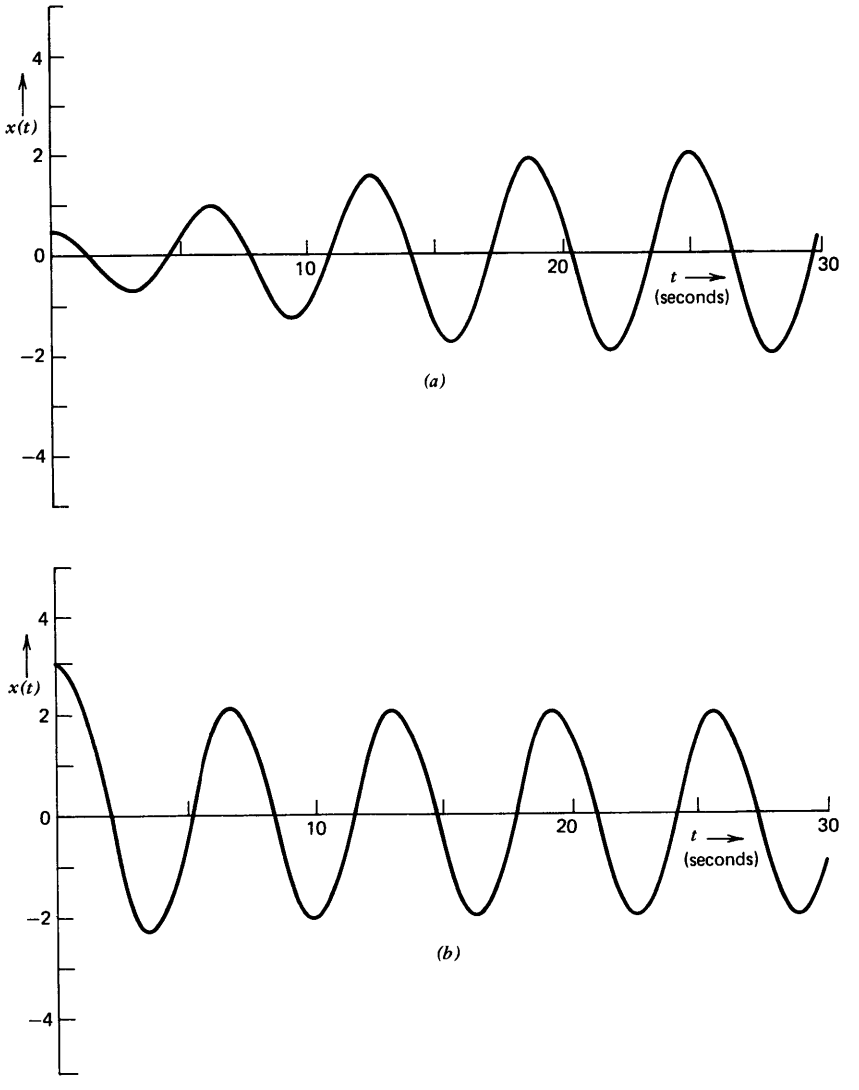


Figure 12.15 Solution to $d^2x/dt^2 + 0.25(x^2 - 1)(dx/dt) + x = 0$. (*a*) With initial conditions $x(0) = 0.5$, $(dx/dt)(0) = 0$. (*b*) With initial conditions $x(0) = 3$, $(dx/dt)(0) = 0$, (*c*) Parts *a* and *b* repeated in phase-plane form.

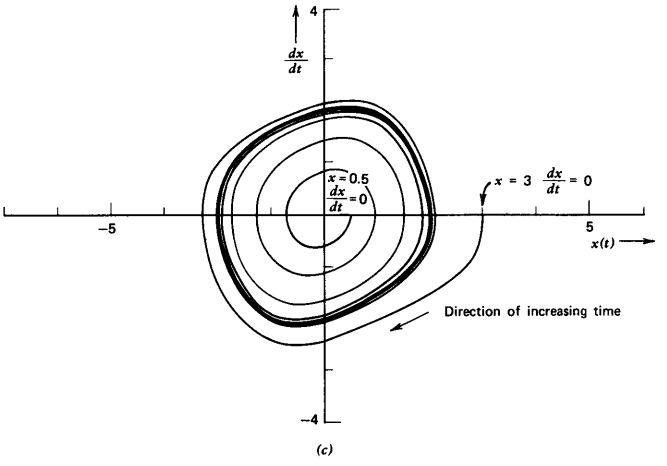


Figure 12.15—Continued

12.3.2 Amplitude and Time Scaling

Practical considerations constrain the amplitude and frequency range of the signals that arise in analog computation. We normally prefer maximum signal levels that are comfortably below amplifier saturation levels, but well above noise and offset uncertainties. Similarly, very low-frequency signals are difficult to integrate accurately, while the limited gain of an operational amplifier at high frequencies compromises accuracy in this frequency range. *Amplitude scaling* and *time scaling* are used to standardize signals to convenient amplitude levels and spectral content.

Amplitude scaling involves little more than some additional bookkeeping effort. Since we are using voltages for all of the dependent variables in our simulation, there must be a dimensioned scale factor that relates the machine variables to the problem variables when the problem variables are quantities other than voltages. For example, if x is a displacement in meters and some voltage in a simulation represents this variable on a 1 meter = 1 volt basis, the machine variable should really be labeled (1 volt/meter)x rather than simply x as is frequently done. We should realize that the number associated with the scale factor can readily be selected to be other than unity. Thus we might use $10x$ as the label for some voltage, or, preferably (10 volts/meter)x. If this voltage were 7 volts, the corresponding displacement would be x = (7 volts) (1 meter/10 volts) = 0.7 meter. The appropriate values for scale factors can only be determined with a knowledge of approximate problem-variable levels, since the corresponding machine variables should have peak values slightly below the saturation

level. Once scale factors have been selected, they are implemented by modifying the gains of amplifiers and integrators from their initially selected values.

Time scaling has advantages beyond those of centering signal-frequency components within the range of optimum operational-amplifier performance. Consider, for example, the simulation of a planetary motion problem that may require years of "real time" to complete. Using a faster "machine time" scale permits us to obtain the solution in a more reasonable time interval. Similarly, the use of a slower than real time scaling procedure allows us to display the buildup of charge in the base region of a transistor at a rate comfortable for viewing on a display oscilloscope.

The technique used for time scaling involves the substitution

$$t = \sigma\tau \tag{12.40}$$

where τ is machine time and is equal to real time divided by a scale factor σ. A value of σ greater than one implies that the machine solution is *faster* than the actual solution so that one second of real time is represented by a shorter period τ of machine time.

This process is illustrated using the form for a differential equation given in Eqn. 12.34 and repeated here for convenience.

$$a_n \frac{d^n x}{dt^n} + a_{n-1} \frac{d^{n-1} x}{dt^{n-1}} + \cdots + a_1 \frac{dx}{dt} + a_0 x = f(t) \tag{12.34}$$

In order to apply the substitution of Eqn. 12.40, we change $f(t)$ to $f(\sigma\tau)$ and change $d^m x/dt^m$ to $(1/\sigma^m)(d^m x/d\tau^m)$. Thus the time-scaled version of Eqn. 12.34 is

$$\frac{a_n}{\sigma^n} \frac{d^n x}{d\tau^n} + \frac{a_{n-1}}{\sigma^{n-1}} \frac{d^{n-1} x}{d\tau^{n-1}} + \cdots + \frac{a_1}{\sigma} \frac{dx}{d\tau} + a_0 x = f(\sigma\tau) \tag{12.41}$$

The equation when simulated will have a solution identical in form to that of Eqn. 12.34, but will run a factor of σ faster than the original equation.

A second way to implement time scaling is to realize that the dynamics of the simulation are implemented by means of integrations, and that changing the scale factor of every integrator in the simulation by some factor must change the time scale of the simulation by precisely the same factor. Thus problems can be time scaled by first simulating the problem for a real-time solution and then dividing the value of every capacitor by a factor of σ. Alternatively, every resistor used to implement all integrators can be reduced in value by a factor of σ, or the scale-factor change can be apportioned between resistors and capacitors. The net result of any of these modifications will be to make the problem on the machine run a factor of σ faster than the real-time solution. It is, of course, still necessary to increase the speed of driving functions applied to the system by a factor of σ if these

signals are derived from sources that are not implemented using scaled integrators.

The coefficients of the original differential equation often can be used to determine the time scale appropriate to a particular problem. If the roots of the characteristic equation have approximately equal magnitudes, the natural frequencies of the undriven solution will be the order of

$$\omega = \left(\frac{a_0}{a_n}\right)^{1/n} \tag{12.42}$$

Conversely, if the system is dominated by one pole, the characteristic frequency is the order of

$$\omega = \frac{a_0}{a_1} \tag{12.43}$$

The characteristic frequencies given by Eqn. 12.42 or 12.43 can be changed to values convenient for display and compatible with operational-amplifier performance by appropriate selection of σ.

The element values that occur in a problem simulation often provide clear indications of the need to modify amplitude or time scales. If, for example, we find that high gain is required at the input of every amplifier being supplied with some particular signal, the scale factor of that signal is probably too small relative to other amplitude scale factors used. Similarly, if one input resistor to a summing amplifier or an integrator is much larger than all other input resistors associated with the amplifier, the implication is that the term applied to the input in question contributes little to the output of the summer or integrator. In the case of time-scale selection, an inappropriate choice is usually reflected by unreasonable resistor values, capacitor values, or both associated with integrators.

The Van der Pol equation simulated earlier (Eqn 12.38) is used as a simple example of time and amplitude scaling. For the range of initial conditions used previously and with $\mu = 0.25$, the maximum magnitudes of x and dx/dt are approximately 3 and 3 $\sec^{-1}$, respectively, while the maximum magnitude of d^2x/dt^2 is slightly greater than 3 $\sec^{-2}$. Accordingly, if 10-volt maximum amplifier outputs are assumed, scale factors of 3 volts per unit for x and dx/dt, combined with a scale factor of 2 volts per unit for d^2x/dt^2 are reasonable. If Eqn. 12.39 is rewritten using these scale factors, we obtain

$$2\frac{d^2x}{dt^2} = -\frac{2}{27}\mu(3x)^2\left(3\frac{dx}{dt}\right) + \frac{2}{3}\mu\left(3\frac{dx}{dt}\right) - \frac{2}{3}(3x) \tag{12.44}$$

The simulation diagram, again assuming that multipliers with outputs equal to the product of the inputs divided by 10 are used, is shown in Fig. 12.16. It has also been assumed in forming this diagram that a voltage

proportional to d^2x/dt^2 is required. Note that the input signals applied to the first amplifier are negatives of the right-hand side of Eqn. 12.44 because of the inversion associated with this amplifier. The transfer function of the first integrator is $-(3/2s)$ so that it provides an output of $-3(dx/dt)$ when driven with $2(d^2x/dt^2)$. Alternate scaling may be advantageous if different values of μ are used to keep the maximum magnitudes of the voltages proportional to dx/dt and d^2x/dt^2 at optimum levels.

If a value of $RC = 1$ second is used, the solution will run at real time, and the oscillation frequency will be about one radian per second. Changing this product will time scale the solution. For example, the use of $RC = 1$ ms results in limit-cycle oscillation at approximately 1000 radians per second.

12.3.3 Ancillary Circuits

There are several interesting circuit configurations that are frequently employed in analog computation and that also can be used in other more general applications.

One of these topologies is the three-mode integrator. We have seen that it is necessary to apply initial conditions to integrators in order to obtain complete (homogeneous plus driven) solutions for simulated differential

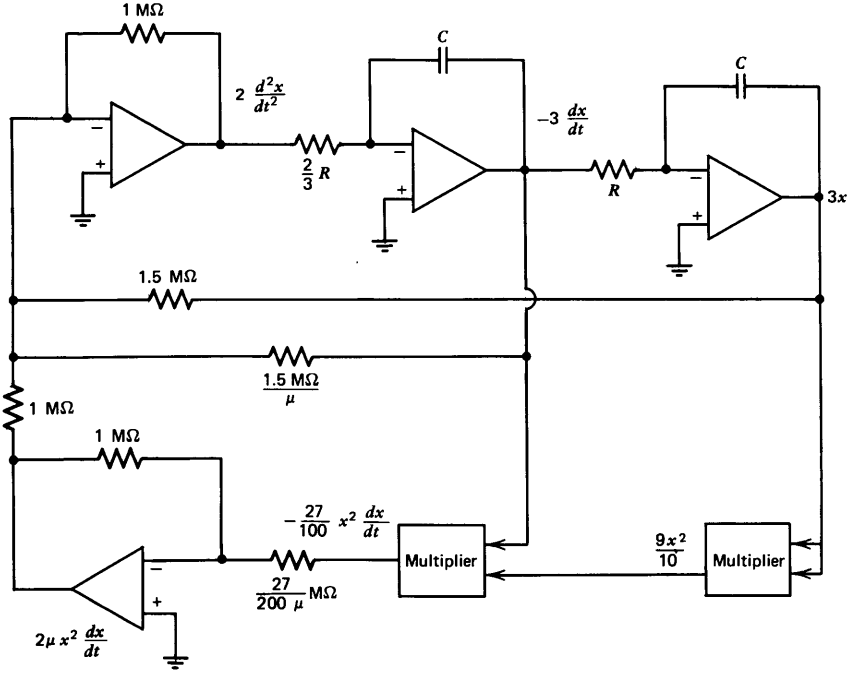


Figure 12.16 Scaled simulation of Van der Pol's equation.

equations. Another useful computing mode results if all integrators are simultaneously switched to a state where their outputs become time invariant and thus hold the values that were present at the switching time. The values of problem variables at the switching time can then be determined accurately with a digital voltmeter.

The three-mode integrator shown in Fig. 12.17 permits application of initial conditions and allows holding an output voltage in addition to functioning as an integrator. The reset (or initial condition), operate, and hold modes are selected by appropriate choice of switch positions. With switch ① open and switch ② closed, the amplifier closed-loop transfer function is

$$\frac{V_o(s)}{V_a(s)} = -\frac{1}{R_2Cs + 1} \tag{12.45}$$

If v_A is time invariant in this mode, the capacitor will charge so that the output voltage eventually becomes the negative of v_A. The capacitor voltage can then provide initial conditions for subsequent operations.

If switch ① is closed and switch ② is open, the amplifier integrates v_B in the usual fashion.

With both switches open, capacitor current is limited to operational-amplifier input current and capacitor self-leakage; thus capacitor voltage is ideally time invariant.

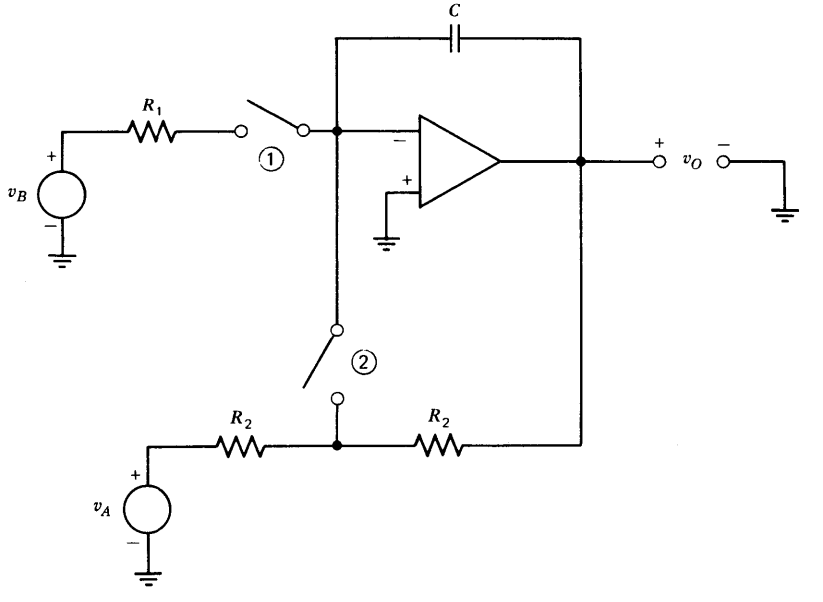


Figure 12.17 Three-mode integrator.

The required reset time of the connection shown in Fig. 12.17 can be quite long if reasonable values are used for the resistors labeled R_2. The use of a second operational amplifier connected as a voltage follower and supplying a low-resistance drive for the inverting input of the integrator can substantially shorten reset times. A practical three-mode integrator circuit that incorporates this feature is shown in Fig. 12.18.

The bipolar-transistor drivers are compatible with T^2L logic signals, and drive the gate potential of field-effect-transistor switches to ground on inputs that exceed two diode forward voltages. With a high level for the "operate" signal and the "reset" signal at ground, Q_1 is on and Q_2 is off. This combination puts the circuit in the normal integrating mode. FET Q_1 has a drain-to-source on resistance of approximately 25 ohms, and this value is compensated for by reducing the integrating-resistor size by a

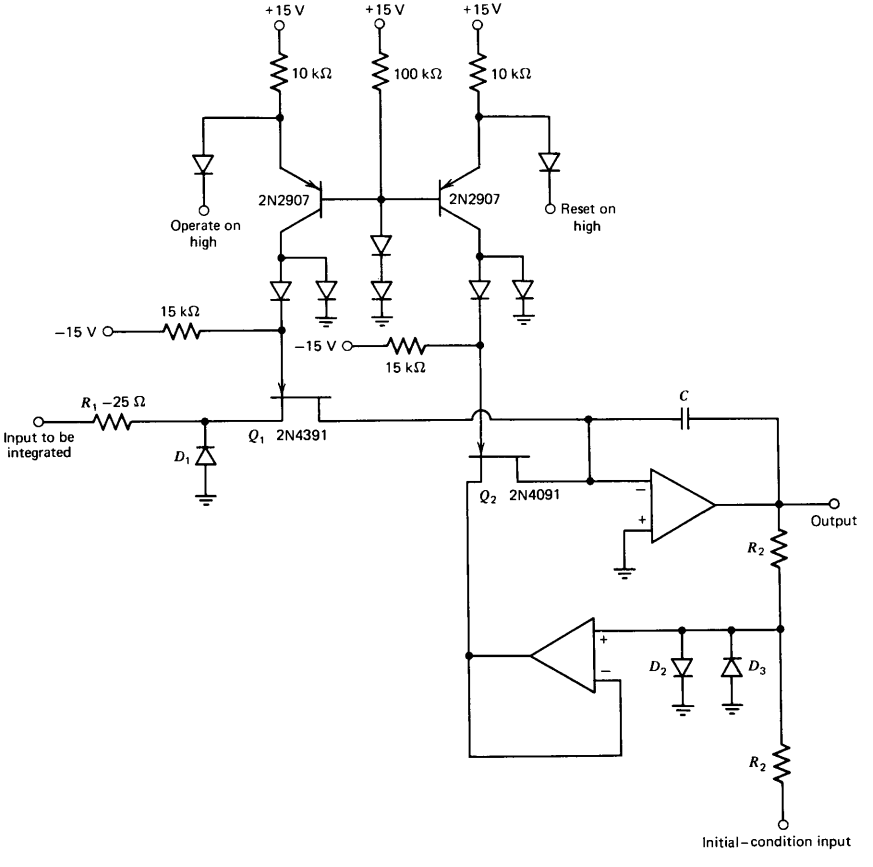


Figure 12.18 Circuit for three-mode integrator.

corresponding amount. Diode D_1 does not conduct significant current in this state. Diodes D_2 and D_3 keep the output of the follower within approximately 0.6 volt of ground. One benefit of this clamping is that the source of Q_2 cannot become negative enough to initiate conduction with its gate at -15 volts, since the maximum pinchoff voltage of the 2N4391 is 10 volts. Clamping the follower input level also keeps its signal levels near those anticipated during reset thus avoiding long slewing periods when the circuit is switched to apply initial conditions.

With the gate of Q_1 at -15 volts (corresponding to a low level on the "operate" control line), diode D_1 prevents source potentials that would initiate conduction of transistor Q_1. If Q_2 is on, the output voltage is driven toward the negative of the initial-condition input-signal level. The details of the transient for a large error depend on diode, FET, and amplifier characteristics. As the error signal becomes smaller, the reset loop enters its linear operating region. The reader should convince himself that the linear-region transmission of the reset loop (assuming ideal operational amplifiers) is $-1/2r_{ds}Cs$, where r_{ds} is the incremental drain-to-source on resistance of the FET. Thus the low FET resistance, rather than R_2, determines linear-region dynamics.

The hold mode results with both the "operate" and the "reset" signals at ground so that both FET's are off. In this state the current supplied to the capacitor is determined by FET leakage and amplifier input current.

One application for this type of circuit in addition to its use in analog computation is as a sample-and-hold circuit. In this case the operate switch is not needed, and the circuit is switched from sampling the negative of an input voltage to hold with Q_2.

Sinusoidal signals are frequently used as test inputs in analog-computer simulations. A quadrature oscillator that includes limiting and that is easily assembled using components available on most analog computers is shown in Fig. 12.19. The diagram implies a simulated differential equation, prior to limiting, of

$$-R^2C^2\frac{d^2v_O}{dt^2} = -\frac{RC}{K}\frac{dv_O}{dt} + v_O \tag{12.46}$$

We recognize this equation as a linear, second-order differential equation with $\omega_n = 1/RC$ and $\zeta = -1/2K$. The value of K is chosen small enough to guarantee oscillation with anticipated capacitor losses and amplifier imperfections, thus insuring that signal amplitudes will be determined primarily by the diode-resistor networks shown.

A precisely known voltage reference is required in many simulations to apply constant input signals, provide initial-condition voltages, function as a bias level for nonlinearities, or for other purposes. Voltage references are also used regularly in a host of applications unrelated to analog simulation.

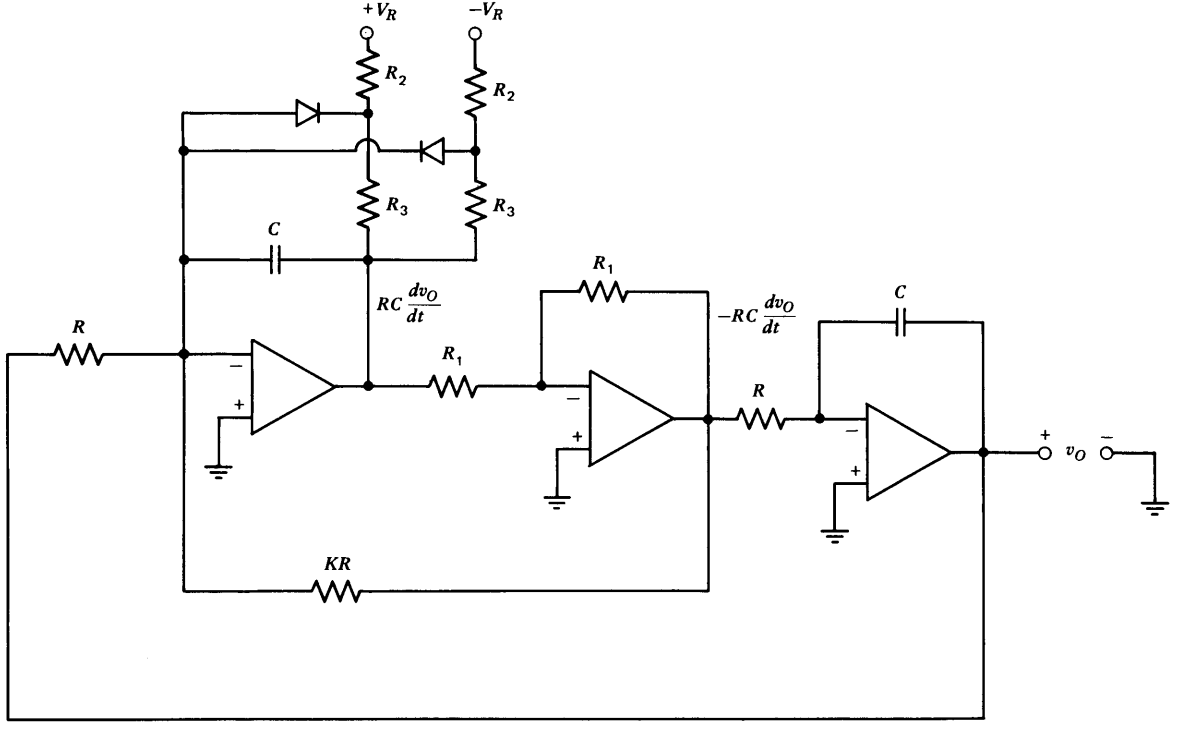


Figure 12.19 Quadrature oscillator with limiting.

The circuit shown in Fig. 12.20 is a simple yet highly stable voltage reference. The operational amplifier is connected for a noninverting gain of slightly more than 1.5 so that a 10-volt output results with 6.4 volts applied to the noninverting amplifier input.

With the topology as shown, the voltage across the resistor connected from the amplifier output to its noninverting input is constrained by the amplifier closed-loop gain to be 0.562 V_Z where V_Z is the forward voltage of the Zener diode. The current through this resister is the bias current applied to the Zener diode. Zener-diode current is thus established by the stable value of the Zener voltage itself. The Zener output resistance does not deteriorate voltage regulation since the diode is operated at constant current in this connection. The filter following the Zener diode helps to attentuate noise fluctuations in its output voltage.

An emitter follower is included inside the operational-amplifier loop to increase output current capacity (current limiting circuitry as discussed in Section 8.4 is often a worthwhile precaution) and to lower output impedance, particularly at higher frequencies. While the low-frequency output impedance of the circuit would be small even without the follower because of feedback, this impedance would increase to the amplifier open-loop output impedance at frequencies above crossover. The emitter follower reduces open-loop output impedance to improve performance when pulsed or high-frequency load-current changes are anticipated. A shunt capacitor at the output may also be used to lower high-frequency output impedance. (See Section 5.2.2.)

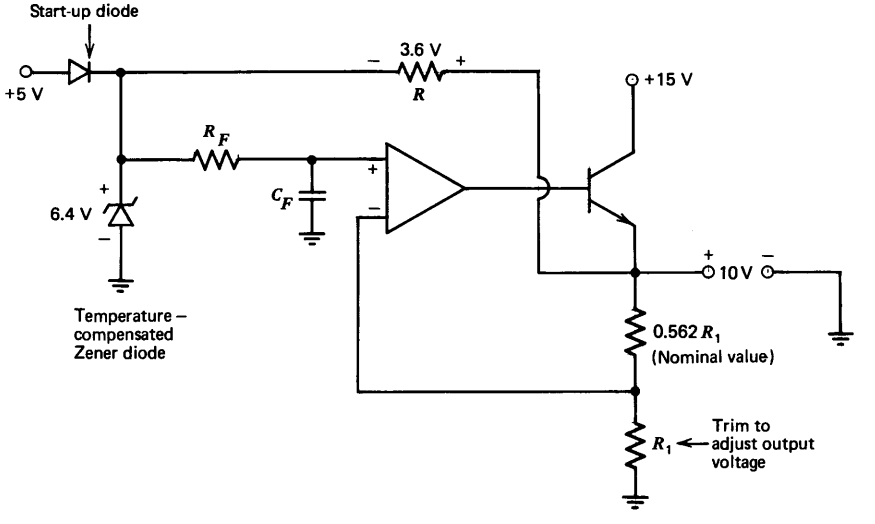


Figure 12.20 Voltage reference.

The bootstrapping used to excite the Zener diode is of course a form of positive feedback and would deteriorate performance if the magnitude of this feedback approached unity. The low-frequency transmission of the positive feedback loop is

$$L = 1.562 \frac{r_d}{R + r_d} \tag{12.47}$$

where r_d is the incremental resistance of the Zener diode. This expression is evaluated using parameters for a 1N829A, a temperature-compensated Zener diode. The diode is designed for an operating current of 7.5 mA, and thus R will be approximately 500 Ω. The incremental resistance of the diode is specified as a maximum of 10 Ω. Thus the loop transmission is, from Eqn. 12.47, 0.03. This small amount of positive feedback does not significantly affect performance.

The positive feedback can result in the circuit operating with the diode in its forward-conducting state rather than its normal reverse-breakdown mode. This state, which leads to a negative output of approximately one volt, can be eliminated with the start-up diode shown. The start-up diode insures that the Zener diode is forced into its reverse region, but does not contribute to Zener current under normal operating conditions.

The expected operational-amplifier imperfections have relatively little effect on the overall performance of the reference circuit. A value of 30,000 for supply-voltage rejection ratio (typical for integrated-circuit amplifiers) causes a change in output voltage of approximately 50 μV per volt of supply change. (This 33 μV/V sensitivity is amplified by the closed-loop gain of 1.5.) The typical input-voltage drift for many inexpensive operational amplifiers is the order of 5 μV per degree Centigrade. This figure is not significant compared to the temperature coefficient of 5 parts per million per degree Centigrade or approximately 32 μV per degree Centigrade of a high-quality Zener diode such as the 1N829A.

The designers of the large analog computers that evolved during the period from the early 1950s to the mid-1960s often devoted almost fanatical effort to achieving high static accuracy in their computing elements. Toward this end, operational amplifiers were surrounded with high-precision wirewound resistors and capacitors that could be accurately trimmed to desired values. These passive components were often placed in temperature-stable ovens to eliminate variations with ambient temperature.

The low-frequency errors (particularly input voltage offset) characteristic of vacuum-tube operational amplifiers were largely eliminated by means of an imaginative technique known as *chopper stabilization*.[5] This method

[5] E. A. Goldberg, "Stabilization of Wide-Band Direct Current Amplifiers for Zero and Gain," *RCA Review*, Vol. II, No. 2, June 1950, pp. 296–300.

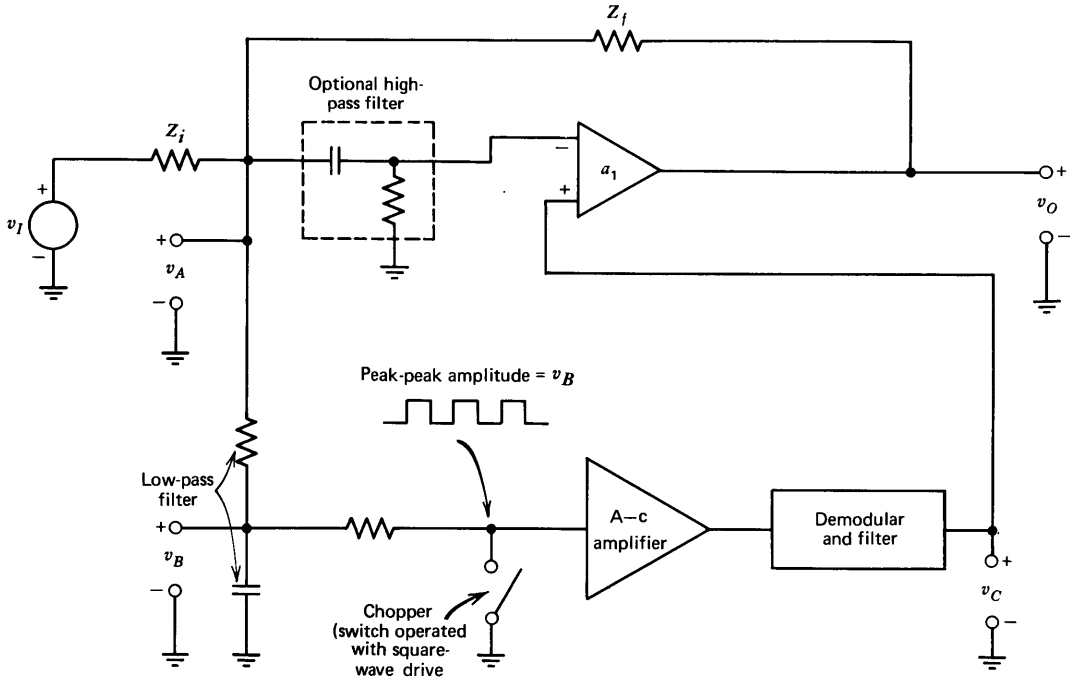


Figure 12.21 Chopper-stabilized amplifier.

is still incorporated into some modern operational-amplifier designs, and it provides a way of reducing the voltage drift and input current of an amplifier to vanishingly small levels. The usual implementation of this technique can be viewed as an extreme example of feedforward (see Section 8.2.2) and thus results in an amplifier that can only be used in inverting connections.

Figure 12.21 illustrates the concept. Assume that the optional network is eliminated so that the junction of Z_f and Z_i is connected directly to the inverting input of the top amplifier. The resulting connection clearly functions as an inverting amplifier if the voltage v_C is zero. Observe that one necessary condition for the amplifier closed-loop gain to be equal to its ideal value is that $v_A = 0$. The objective of chopper stabilization is to reduce v_A to nearly zero by applying an appropriate signal to the noninverting input of the top amplifier.

The d-c component of the voltage v_A is determined with a low-pass filter, and this component (v_B) is "chopped" (converted to a square wave with peak-to-peak amplitude v_B) using a periodically operated switch. (Early designs used vibrating-reed mechanical switches, while more modern units often use periodically illuminated photoresistors or field-effect transistors as the switch.) The chopped a-c signal can be amplified without offset by an a-c amplifier and demodulated to produce a signal v_C proportional to v_B. If the gain of the a-c amplifier is high, the low-frequency gain $v_C/v_A = a_{02}$ will be high. If a_{02} is negative, the signal applied to the positive gain input of the top amplifier will be of the correct polarity to drive v_A toward zero. Arbitrarily small d-c components of v_A can theoretically be obtained by having a sufficiently high magnitude for a_{02}, although in practice achievable offsets are limited by errors such as thermally induced voltages in the switch itself. The low-pass filter is necessary to prevent sampling errors that arise if signals in excess of half the chopping frequency are applied to the chopper.

An alternative way to view the operation of a chopper-stabilized amplifier is to notice that high-frequency signals pass directly through the top amplifier, while components below the cutoff frequency of the low-pass filter are amplified by both the bottom amplifier and the top amplifier in cascade. (It is interesting to observe that low-frequency open-loop gain magnitudes in excess of 10^9 have been achieved in this way.) It is therefore not necessary to apply low-frequency signals directly to the top amplifier, and a high-pass filter (shown as the optional network) can be included in series with the inverting input of the top amplifier. As a result, both voltage offset and input current to the operational amplifier can be reduced by chopper stabilization, yielding an amplifier with virtually ideal low-frequency characteristics.

Several manufacturers offer packages that combine discrete-component choppers with integrated-circuit amplifiers. More recently, integrated-

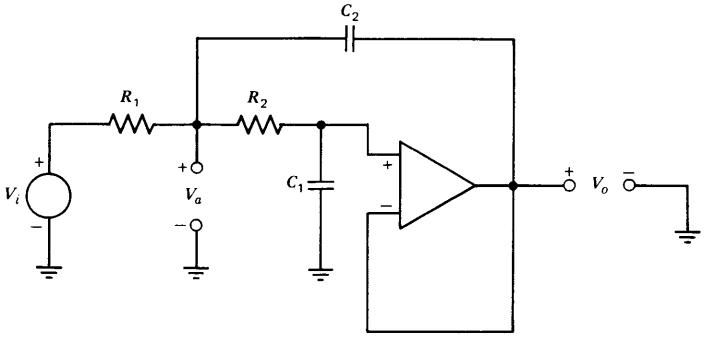


Figure 12.22 Second-order low-pass active filter.

circuit manufacturers have been able to fabricate complete chopper-stabilized amplifiers either in monolothic form or by combining several monolithic chips to form a hybrid circuit. These circuits incorporate topological improvements that permit true differential operation. The large capacitors required are connected externally to the package. Drifts of a fraction of a microvolt per degree Centigrade, coupled with input currents in the picoampere range, are available at surprisingly low cost.

12.4 ACTIVE FILTERS

There are numerous applications that require the realization of a particular transfer function. One of the many limitations of the design of filter networks using only passive components is that inductors are required to obtain complex pole locations. This restriction is removed if active elements are included in the designs, and the resultant *active filters* permit the realization of complex poles using only resistors and capacitors in addition to the active elements. Further advantages of active-filter synthesis include the possibility of a wide range of relative input and output impedances, and the use of smaller, less expensive reactive components than is normally possible with passive designs.

There is a fair amount of present research devoted toward improving techniques for active-filter synthesis, and the probability is that better designs, particularly with respect to *sensitivity* (the dependence of the transfer function on variations in parameter values), will evolve. This section describes two presently popular topologies that can be used to realize active filters.

12.4.1 The Sallen and Key Circuit[6]

Figure 12.22 shows an active-filter circuit that uses a unity-gain-connected operational amplifier. Node equations for the circuit are easily

[6] R. P. Sallen and E. L. Key, "A Practical Method of Designing RC Active Filters," Institute of Radio Engineers, *Transactions on Circuit Theory*, March, 1955, pp. 74–85.

written by noting that the voltage at the noninverting input of the amplifier is equal to the output voltage and are

$$G_1V_i = (G_1 + G_2 + C_2s)V_a - (G_2 + C_2s)V_o \tag{12.48}$$
$$0 = -G_2V_a + (G_2 + C_1s)V_o$$

Solving for the transfer function yields

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{R_1R_2C_1C_2s^2 + (R_1 + R_2)C_1s + 1} \tag{12.49}$$

This equation represents a second-order transfer function with standard-form parameters

$$\omega_n = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{12.50}$$

and

$$\zeta = \frac{R_1 + R_2}{2\sqrt{R_1R_2}} \sqrt{\frac{C_1}{C_2}} \tag{12.51}$$

Since only two quantities are required to characterize the second-order filter, the four degrees of freedom represented by the four passive-component values are redundant. Part of this redundancy is frequently eliminated by choosing $R_1 = R_2 = R$. In this case, the standard-form parameters become

$$\omega_n = \frac{1}{R\sqrt{C_1C_2}} \tag{12.52}$$

and

$$\zeta = \sqrt{\frac{C_1}{C_2}} \tag{12.53}$$

The addition of another section to the second-order low-pass active filter as shown in Fig. 12.23 allows the synthesis of a third-order transfer function with a single amplifier. If equal-value resistors are used as shown, the transfer function is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{C_1C_2C_3R^3s^3 + 2(C_1C_3 + C_2C_3)R^2s^2 + (C_1 + 3C_3)Rs + 1} \tag{12.54}$$

An nth-order low-pass filter is often designed by combining $n/2$ second-order sections in the case of n even, or one third-order section with $n/2 - 3/2$ second-order sections when n is odd. Tables[7] that simplify

[7] Farouk Al-Nasser, "Tables Speed Design of Low-Pass Active Filters," *EDN*, March 15, 1971, pp. 23–32.

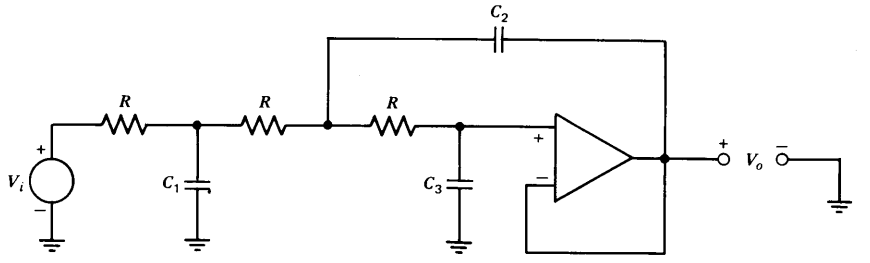


Figure 12.23 Third-order low-pass active filter.

element-value selection are available for filters up to the tenth order with a number of different pole patterns.

Interchanging resistors and capacitors as shown in Fig. 12.24 changes the second-order low-pass filter to a high-pass filter. The transfer function for this configuration is

$$\frac{V_o(s)}{V_i(s)} = \frac{R_1R_2C_1C_2s^2}{R_1R_2C_1C_2s^2 + R_2(C_1 + C_2)s + 1} \tag{12.55}$$

If, in a development analogous to that used for the low-pass filter, we choose $C_1 = C_2 = C$, Eqn. 12.55 reduces to

$$\frac{V_o(s)}{V_i(s)} = \frac{s^2/\omega_n^2}{(s^2/\omega_n^2) + (2\zeta s/\omega_n) + 1} \tag{12.56}$$

where

$$\omega_n = \frac{1}{C\sqrt{R_1R_2}}$$

and

$$\zeta = \sqrt{\frac{R_2}{R_1}}$$

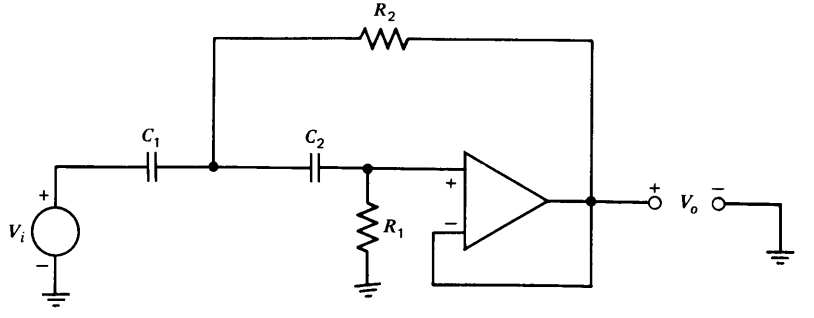


Figure 12.24 Second-order high-pass active filter.

The Sallen and Key circuit can be designed with an amplifier gain other than unity (see Problem P12.8). This modification allows greater flexibility, since the low- or high-frequency gain of the circuit can be made other than one. However, the damping ratio of transfer functions realized in this way is dependent on the values of resistors that set the closed-loop amplifier gain; thus poles may be somewhat less reliably located. A further advantage of the unity-gain version is that it may be constructed using the LM110 integrated circuit (see Section 10.4.4). The bandwidth of this amplifier far exceeds that of most general-purpose integrated-circuit units, and corner frequencies in the low megahertz range can be obtained using it.

12.4.2 A General Synthesis Procedure

The Sallen and Key configuration, together with many other active-filter topologies, allows complete freedom in the choice of pole location, but does not permit arbitrary placement of transfer-function zeros. The application of the analog-computation concepts described in Section 12.3.1 allows the synthesis of any realizable transfer function that is expressable as a ratio of polynomials in s, provided that the number of poles is equal to or greater than the number of zeros in the transfer function.

Consider the transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_1 s + b_0}{a_n s^n + a_{n-1}s^{n-1} + \cdots + a_1 s + a_0} \tag{12.57}$$

The first step is to introduce an intermediate variable $V_a(s)$ such that $V_a(s)/V_i(s)$ contains only the poles of the transfer function, or

$$\frac{V_a(s)}{V_i(s)} = \frac{1}{a_n s^n + a_{n-1}s^{n-1} + \cdots + a_1 s + a_0} \tag{12.58}$$

Proceeding in a way exactly parallel to the time-domain development of Section 12.3.1, we write

$$s^n V_a(s) = -\frac{a_{n-1}}{a_n} s^{n-1} V_a(s) - \cdots - \frac{a_1}{a_n} s V_a(s) - \frac{a_0}{a_n} V_a(s) + \frac{V_i(s)}{a_n} \tag{12.59}$$

The block-diagram representation of Eqn. 12.59 is shown in Fig. 12.25. This block diagram can be readily implemented using summers and integrators. In order to complete the synthesis of our transfer function (Eqn. 12.57) we recognize that

$$V_o(s) = V_a(s)\,(b_n s^n + b_{n-1}s^{n-1} + \cdots + b_1 s + b_0) \tag{12.60}$$

The essential feature of Eqn. 12.60 is that it indicates $V_o(s)$ is a linear combination of $V_a(s)$ and its first n derivatives. Since all of the necessary vari-

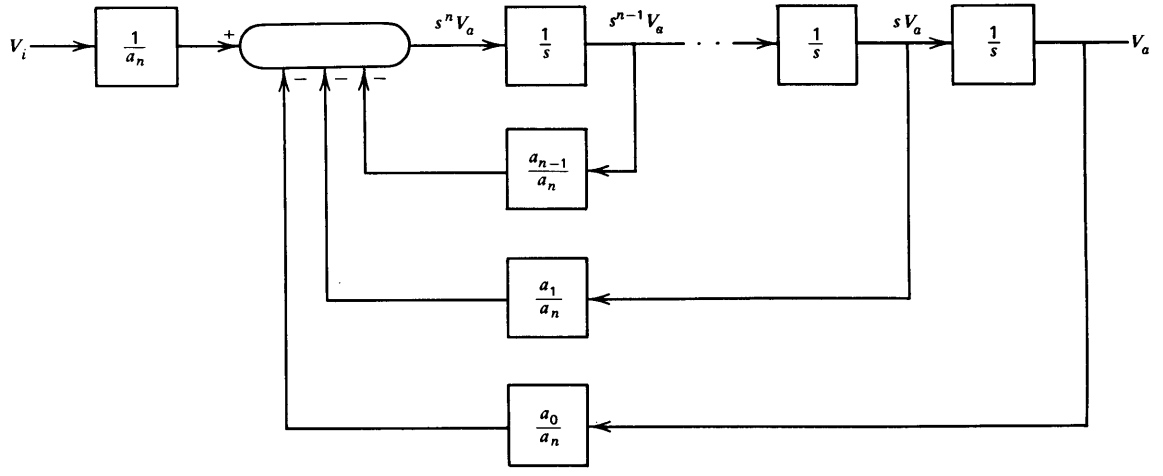


Figure 12.25 Block diagram representation of transfer function that contains only poles.

ables appear in the block diagram, $V_o(s)$ can be generated by simply scaling and summing these variables, without the need for differentiation.

This synthesis procedure is illustrated for an approximation to a pure time delay known as the Padé approximate. The time delay has a transfer function $e^{-s\tau}$, where τ is the length of the delay. The magnitude of this transfer function is one at all frequencies, while its negative phase shift is linearly proportional to frequency. The time delay has an essential singularity at the origin, and thus cannot be exactly represented as a ratio of polynomials in s.

The Taylor's series expansion of $e^{-s\tau}$ is

$$e^{-s\tau} = 1 - s\tau + \frac{s^2\tau^2}{2!} - \cdots + \cdots + (-1)^m \frac{s^m\tau^m}{m!} + \cdots \quad (12.61)$$

The Padé approximates locate an equal number of poles and zeros so as to agree with the maximum possible number of terms of the Taylor's series expansion. This approximation always leads to an *all-pass network* that has right-half-plane zeros and left-half-plane poles located symmetrically with respect to the imaginary axis. This type of singularity pattern results in a frequency-independent magnitude for the transfer function.

Since we can always frequency or time scale at a later point, we consider a unit time delay e^{-s} to simplify the development. The first-order Padé approximate to this function is

$$P_1(s) = \frac{1 - (s/2)}{1 + (s/2)} = 1 - s + \frac{s^2}{2} - \frac{s^3}{4} + \cdots - \cdots + \quad (12.62)$$

The expansion for e^{-s} is

$$e^{-s} = 1 - s + \frac{s^2}{2} - \frac{s^3}{6} + \frac{s^4}{24} - \frac{s^5}{120} + \frac{s^6}{720} - \cdots + \quad (12.63)$$

The first-order approximation matches the first two coefficients of s of the complete expansion, and is in reasonable agreement with the third coefficient. This match is all that can be expected, since only two degrees of freedom (the location of the pole and the location of the zero) are available for the first-order approximation. The second-order Padé approximate to a one-second time delay is

$$P_2(s) = \frac{1 - (s/2) + (s^2/12)}{1 + (s/2) + (s^2/12)}$$

$$= 1 - s + \frac{s^2}{2} - \frac{s^3}{6} + \frac{s^4}{24} - \frac{s^5}{144} + \cdots - \cdots + \quad (12.64)$$

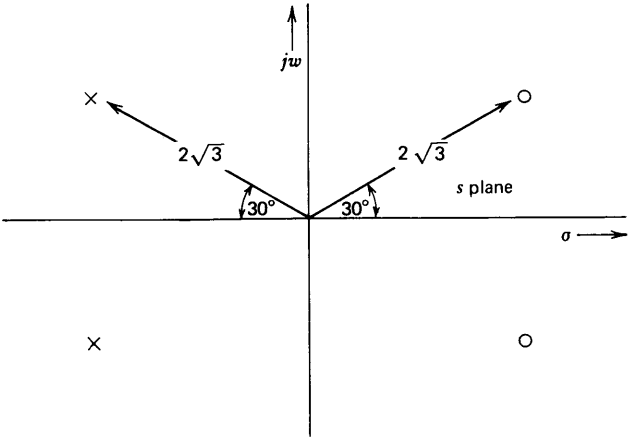


Figure 12.26 Singularity locations for second-order Padé approximate to one-second time delay.

As expected, the first four time-delay coefficients of s are matched by the approximation. The s-plane plot for $P_2(s)$ is shown in Fig. 12.26. Simple vector manipulations confirm the fact that the magnitude of this function is one at all frequencies.

The phase shift of the approximating function is (from Eqn. 12.64)

$$\measuredangle P_2(j\omega) = 2 \measuredangle \left[1 - \frac{j\omega}{2} + \frac{(j\omega)^2}{12}\right] = -2 \tan^{-1} \left\{\frac{\omega}{2[1 - (\omega^2/12)]}\right\} \quad (12.65)$$

This function is compared with an angle of $-57.3°\omega$ (the value for a one-second time delay) in Fig. 12.27. We note excellent agreement to frequencies of approximately 2 radians per second implying that the approximation represents the actual function well for sinusoidal excitation to this frequency, with increasing discrepancy at higher frequencies. The error reflects the fact that the maximum negative phase shift of the Padé approximate is 360°, while the time delay provides unlimited negative phase shift at sufficiently high frequency.

Synthesis is initiated by defining an intermediate variable $V_a(s)$ in accordance with Eqns. 12.58 and 12.59, or

$$\frac{V_a(s)}{V_i(s)} = \frac{1}{(s^2/12) + (s/2) + 1} \quad (12.66)$$

and

$$s^2 V_a(s) = -6sV_a(s) - 12V_a(s) + 12V_i(s) \quad (12.67)$$

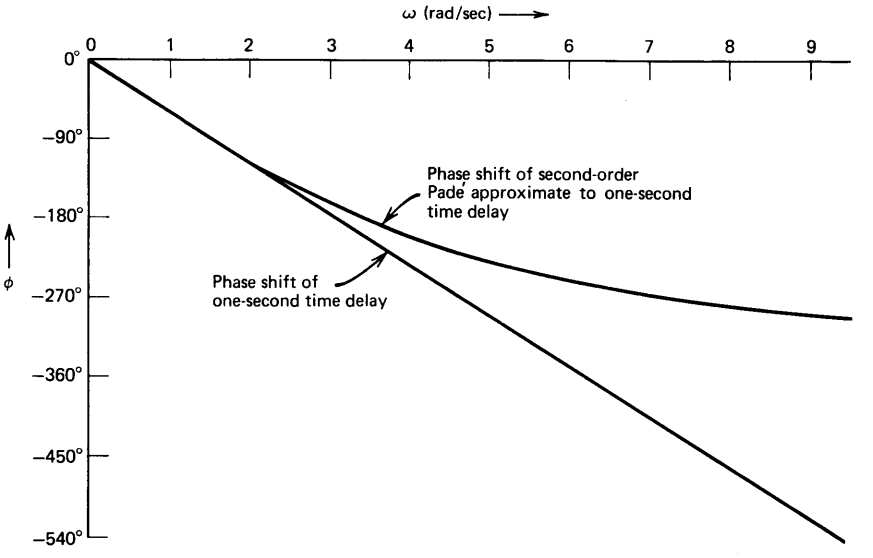


Figure 12.27 Comparison of time delay and Padé approximate phase characteristics.

The output voltage is

$$V_o(s) = \frac{s^2}{12} V_a(s) - \frac{s}{2} V_a(s) + V_a(s) \tag{12.68}$$

The operational-amplifier synthesis shown in Fig. 12.28 provides the required transfer function if $RC = 1$ second. The reader should convince himself that the liberties taken with inversions and various resistor values do in fact lead to the desired relationship.

Anticipated amplitudes depend on the input-signal level and its spectral content. For example, if a step is applied to the input of the circuit, the magnitude of the signal out of the first amplifier must initially be 12 times as large as the step amplitude, since the outputs of the integrators cannot change instantaneously to subtract from the input-signal level. Note, however, that the input-to-output transfer function of the circuit remains the same for any values of $R_1 = R_2$. If, for example, 10-V step changes are expected at the input, selection of $R_1 = R_2 = 120$ kΩ will limit the signal level at the output of the first amplifier to 10 volts while maintaining the correct input-to-output gain.

The circuit shown in Fig. 12.28 was constructed using $R = 100$ kΩ and $C = 0.01$ μF, values resulting in an approximation to a 1-ms time delay. This choice of time scale is convenient for oscilloscope presentation. The

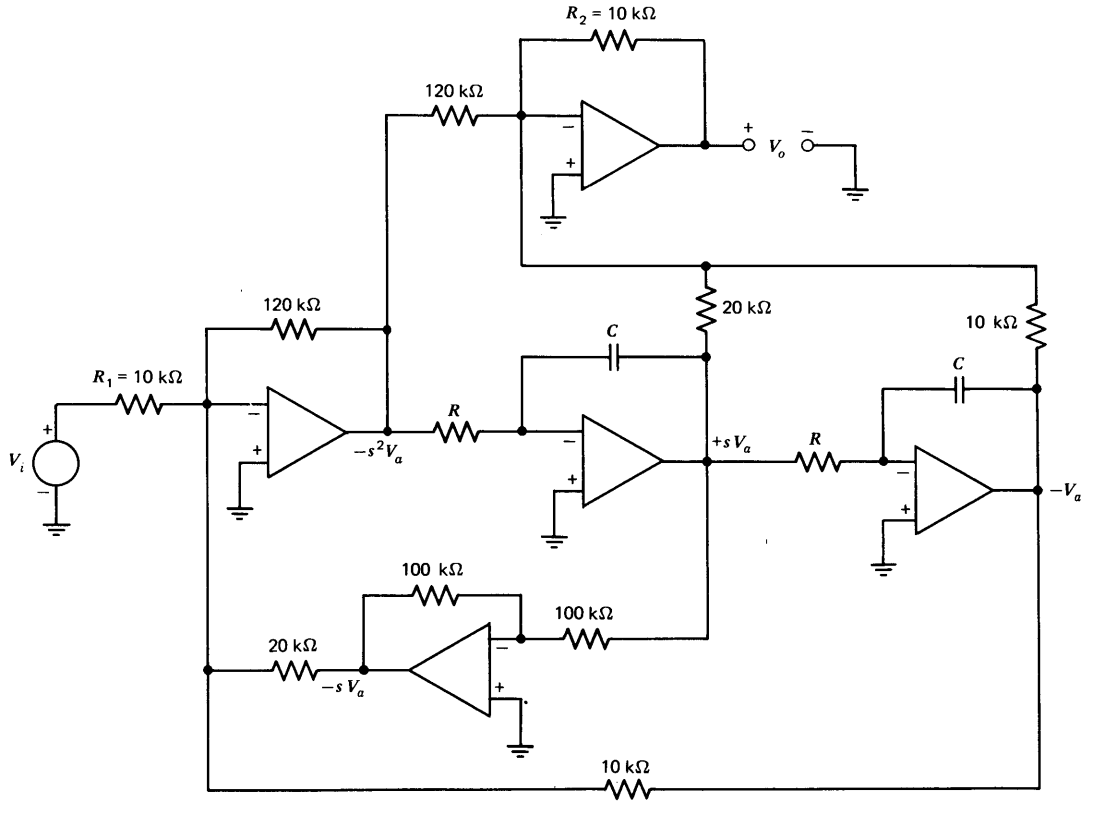


Figure 12.28 Synthesis of second-order Padé approximate to a time delay.

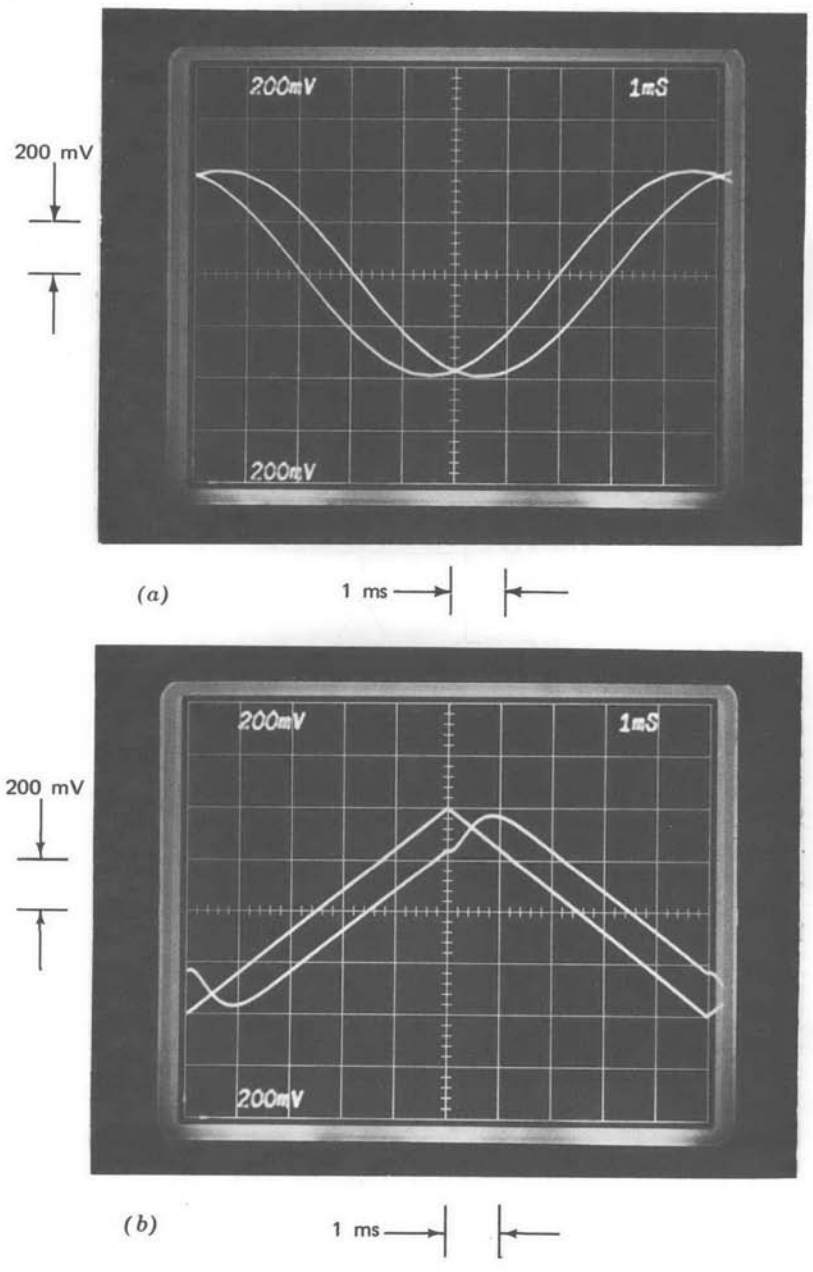


Figure 12.29 Input and output signals for second-order Padé approximate to a 1-ms time delay. (*a*) Sine-wave excitation. (*b*) Triangular-wave excitation. (*c*) Square-wave excitation.

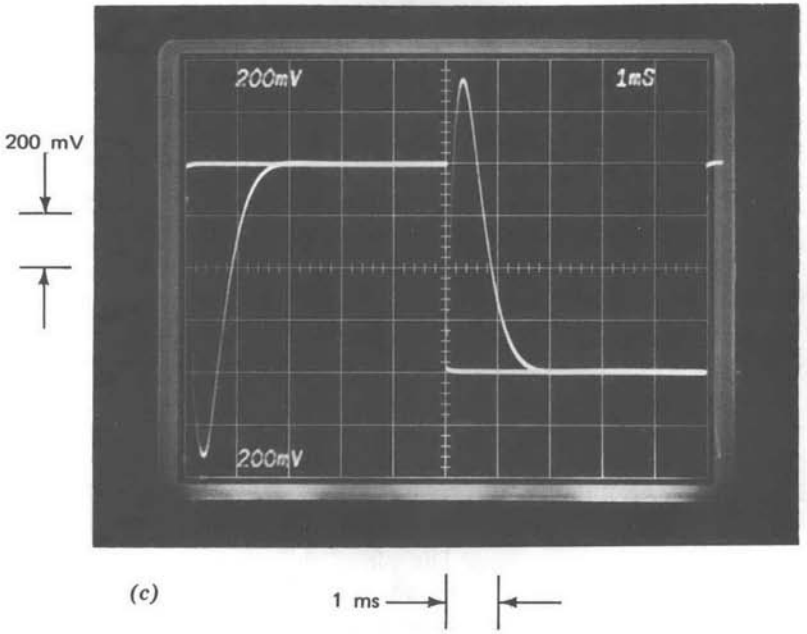


Figure 12.29—Continued

input and output signals for 100-Hz sine-wave excitation are shown in Fig. 12.29*a*. The time delay between these two signals is 1 ms to within instrumentation tolerances. This performance reflects the prediction of Fig. 12.27, since good agreement to 2000 rad/sec or 300 Hz is anticipated for the approximation to a 1-ms delay.

Input and output signals for 100-Hz triangular-wave excitation are compared in Fig. 12.29*b*. The triangular wave contains only odd harmonics, and these harmonics fall off as the square of their frequency. Thus the amplitude of the third harmonic of the triangular wave is approximately 11% of the amplitude of the fundamental, the amplitude of the fifth harmonic is 4% of the fundamental, while higher harmonics are further attentuated. We notice that the circuit does very well in approximating a 1-ms time delay most of the time. The aberration that results immediately following a change in slope reflects the inability of the circuit to provide proper phase shift to the higher-frequency components.

The performance of the circuit when excited with an 100-Hz square wave is shown in Fig. 12.29*c*. The relatively poorer behavior in the vicinity of a transition in this case results from the higher harmonic content of the square wave. (Recall that the square wave contains odd harmonics that fall off only as the first power of the frequency.)

12.5 FURTHER EXAMPLES

It was mentioned in the introduction to Chapter 11 that the objective of the application portion of this book was to illustrate concepts for design rather than to provide specific, detailed examples in the usually futile hope that the reader could apply them directly to his own problems. Successful design almost always involves combining bits and pieces, a concept here, a topology there, to ultimately arrive at the optimum solution. In this section we will see how some of the ideas introduced earlier are combined into relatively more sophisticated configurations. The three examples that are presented are all "real world" in that they reflect actual requirements that the author has encountered recently in his own work.

12.5.1 A Frequency-Independent Phase Shifter

There are a number of operational-amplifier connections, such as the approximation to a time delay described in the previous section, that have a transfer-function magnitude independent of frequency combined with specified phase characteristics. The phase shifter shown in Fig. 12.30 is another example of this type of circuit. We recognize this circuit as a differential-amplifier connection, and thus realize that its transfer function is

$$\frac{V_o(s)}{V_i(s)} = \left(\frac{2RCs}{RCs + 1} - 1\right) = \frac{RCs - 1}{RCs + 1} \tag{12.69}$$

This transfer function (which is the negative of a first-order Padé approximate to a time delay of $2RC$ seconds) produces a phase shift that varies from $-180°$ at low frequencies to $0°$ at high frequencies. If a potentiometer or a field-effect transistor is used for R, the phase shift can be manually or electronically varied.

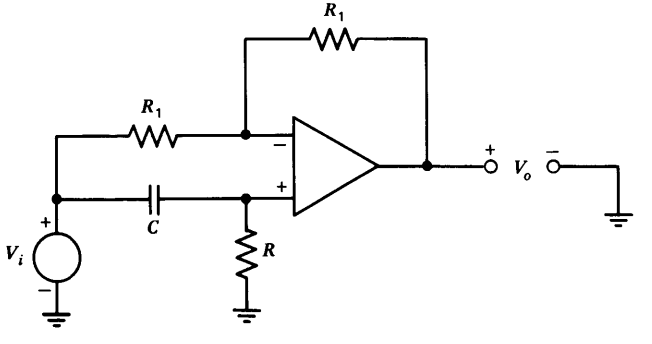


Figure 12.30 Adjustable phase shifter.

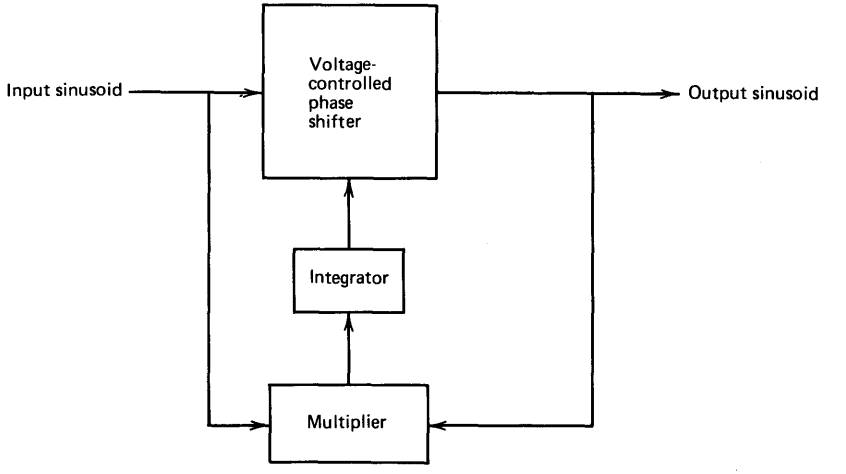


Figure 12.31 Constant phase shifter using a phase detector.

One technique for converting resolver[8] signals to digital form requires that a fixed 90° phase shift be applied to a sinusoidal signal with no change in its amplitude. The frequency of the signal to be phase shifted may change by a few percent. Unfortunately, there are no finite-polynomial linear transfer functions that combine frequency-independent magnitude characteristics with a constant 90° phase shift. While approximating functions do exist over restricted frequency ranges, the arc-minute phase-shift constancy required in this application precluded the use of such functions. We note that since a very specific class of input signals (single-frequency sinusoids) is to be applied to the phase shifter, linearity may not be a necessary constraint. Nonlinear circuits, in spite of our inability to analyze them systematically, often have very interesting properties.

Consider the configuration shown diagrammatically in Fig. 12.31 as a possible solution to our problem. In this circuit, an all-pass phase shifter with a voltage-variable amount of phase shift is the central element. The circuit shown in Fig. 12.30 with a field-effect transistor used for the resistor R can perform this function. The multiplier is used as a phase detector. If the magnitude of the phase shift between the input and output signals is less than 90°, the average value of the multiplier output will be positive, while if this magnitude is between 90° and 180°, the average multiplier output signal will be negative. The integrator, which provides the control

[8] A resolver is basically a transformer with a primary-to-secondary coupling that can be varied by mechanically changing the relative alignment of these windings. This device is used as a rugged and highly accurate mechanical-angle transducer.

voltage for the FET in the phase shifter, filters the second harmonic that results from the multiplication and supplies the loop gain necessary to keep the average value of the multiplier output at zero, thus forcing a 90° phase shift between input and output signals. Although the circuit described above can result in moderate accuracy, a detailed investigation indicated that meeting the required specifications probably was not practical with this topology.

It is worth noting that while the basic approach described above was not used in this case, it is a valuable technique that has a number of interesting and useful variations. For example, the phase shift of a second-order high- or low-pass active filter is $\pm 90°$ when excited at its corner frequency. Tracking filters can be realized by replacing the fixed resistors in an active filter with voltage-controlled resistors and using a phase comparison to locate the corner frequency of the filter at its excitation frequency.

In some applications, other types of phase detectors are used. One possibility involves high-gain limiters that produce square waves with zero crossing synchronized to those of the sine waves of interest. The duty cycle of an exclusive OR gate operating on the square waves indicates the relative phase of the original signals.

The previous circuit combined an all-pass network that provides a transfer-function magnitude that is independent of frequency with feedback which forces 90° of phase shift at the operating frequency. An alternative approach is to combine a network that provides 90° of phase shift at all frequencies (an integrator) with feedback that forces its gain magnitude to be one at the operating frequency.

The circuit that evolved to implement the above concept is shown in only slightly simplified form in Fig. 12.32. The signal integrator provides the required 90° of phase shift. Its scale factor is adjusted by means of the field-effect transistor so that a gain magnitude of one is provided at frequencies close to the nominal operating value of 400 Hz. Half of the drain-to-source voltage of the field-effect transistor is applied to its gate to linearize the drain-to-source resistance as described in Section 12.1.4. The unity-gain buffer amplifier prevents current flowing through the FET-gate network from being integrated. The capacitor in series with the signal-integrator input resistor and the resistor shunting the integrating capacitor are required to keep this integrator from saturating as a consequence of input voltage offset and bias current. While they change the ideal phase shift by a total of approximately eight arc minutes, this value is trimmed out along with other phase-shift errors with a network (not shown) following the integrator.

The two full-wave precision-rectifier connections combine with the loop-gain integrator to provide an average current into the capacitor of this

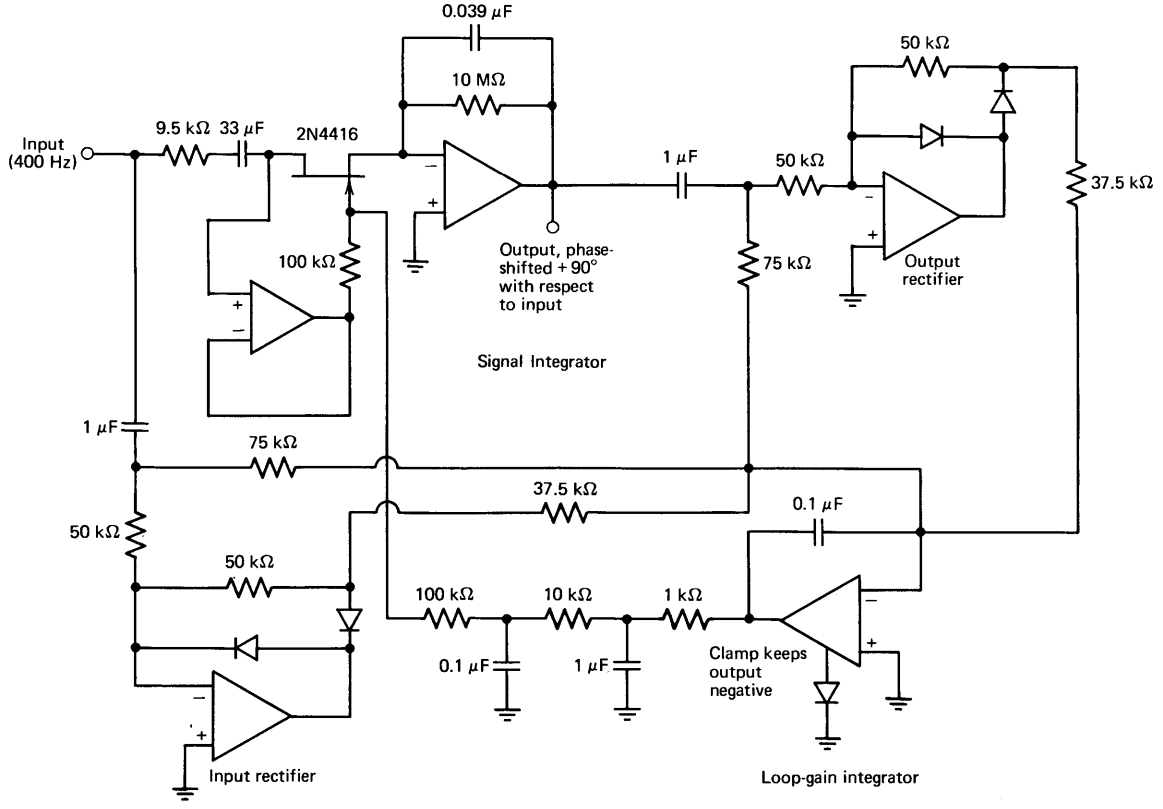


Figure 12.32 Precision phase shifter with amplitude control.

integrator that is proportional to the difference between the magnitudes of the input and output signals. If, for example, the output-signal magnitude exceeds the input-signal magnitude, the voltage out of the loop-gain integrator is driven negative. This action increases the incremental resistance of the FET, thus decreasing the signal-integrator scale factor and lowering the magnitude of the output signal. The inputs to the precision rectifiers are a-c coupled so that d-c components of these signals do not influence the rectifier output signals. A two-pole low-pass filter follows the loop-gain integrator to further filter harmonics that would degrade signal-integrator performance.

The maximum positive output level of the loop-gain integrator is clamped via an internal node to a maximum output level of zero volts in order to eliminate a latch-up mode. If this voltage became positive, the FET would conduct gate current, and this current could cause the signal-integrator output to saturate. As a result, the a-c component of the signal-integrator output would be eliminated, and the loop, in an attempt to restore equilibrium, would drive the output of the loop-gain integrator further positive. The diode clamp prevents initiation of this unfortunate chain of events.

The circuit shown in Fig. 12.32 has been built and tested at operating frequencies between 395 and 405 Hz over the temperature range of 0° to 50° Centigrade. (The feedback also eliminates the effects of signal-integrator component-value changes with temperature.) The input- and output-signal amplitudes remain equal within 1 mV peak-to-peak at any input-signal level up to 20 volts peak-to-peak. The phase shift of the circuit with a 20-volt peak-to-peak input remains constant within one arc minute. While the actual phase shift is not precisely 90°, the constant component of the phase error can be trimmed out as described earlier.

12.5.2 A Sine-Wave Shaper

We have discussed certain aspects of a function-generator circuit that combines an integrator and a Schmitt trigger to produce square and triangle waves in Sections 6.3.3 and 12.2.1. Commercial versions of this circuit usually also provide a sine-wave output that is synthesized by the seemingly improbable method of shaping the triangle wave with a piecewise-linear network. This technique is practical because of the ease of generating variable-frequency triangular waves, and because the use of relatively few segments in the shaping network gives surprisingly good sine-wave fidelity.

Part of the design problem is to determine how the characteristics of the shaping network should be chosen to best approximate a sine wave. The parameters that define the network are shown in Fig. 12.33. A total of n break points are located over the input-variable range of 0° to 90°. The

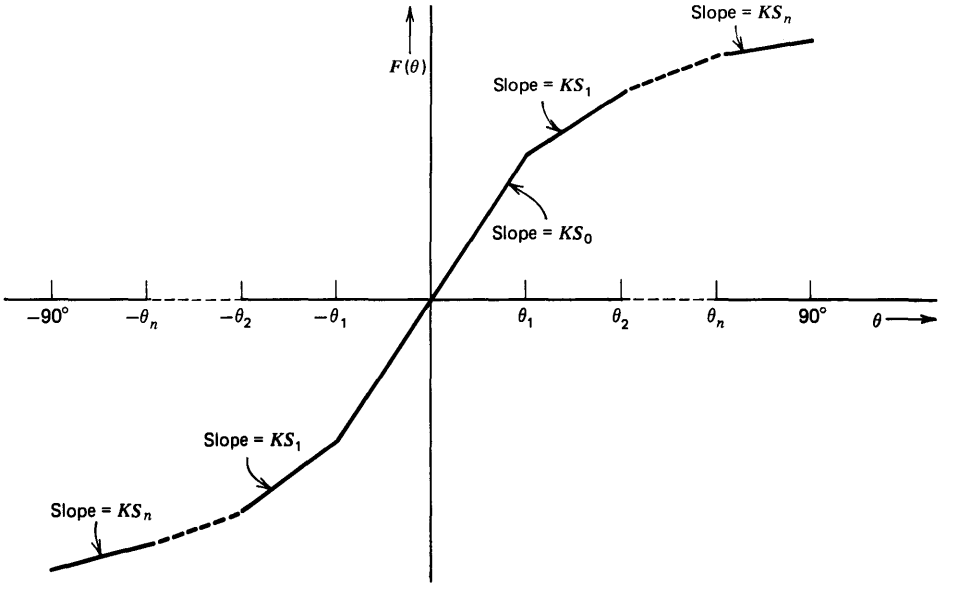


Figure 12.33 Piecewise-linear network characteristics.

slope of the input-output transfer relationship is KS_m between $\theta = \theta_m$ and $\theta = \theta_{m+1}$. The multiplying constant K reflects the fact that only relative slopes are important, since a multiplicative change in all slopes changes only the magnitude of the input-output transfer characteristics. The symmetry of the transfer characteristics about the origin insures that the output signal will have no d-c component and will contain no even harmonics when a zero-average-value triangular signal is used as the input.

The network specification involves the choice of n values of θ (the break-point locations) and $n + 1$ relative slopes. It can be shown that if the θ's are selected such that

$$\theta_m = \frac{m\ 180°}{2n + 1} \qquad 0 \leq m \leq n \tag{12.70}$$

and slopes selected as

$$S_m = \sin \theta_{m+1} - \sin \theta_m \qquad 0 \leq m < n \tag{12.71a}$$

$$S_m = 0 \qquad m = n \tag{12.71b}$$

the first n odd harmonics will be eliminated from the output signal.

The decision to use four break points in the realization of the sine shaper was based on two considerations. With this number of break points, out-

put distortion resulting from imprecise break-point locations and slope values is comparable to the distortion associated with the piecewise-linear approximation unless expensive components are used to establish these parameters. Furthermore, an inexpensive integrated-circuit five-diode array is available. This matched-diode array can be used for the four break points, with the fifth diode providing temperature compensation as described in material to follow. Equations 12.70 and 12.71 evaluated for $n = 4$ suggest break points located at input-variable values of 20°, 40°, 60°, and 80°, with relative segment slopes (normalized to a minimum nonzero slope of one) of 2.879, 2.532, 1.879, 1, and 0, respectively.

With the transfer characteristics of the shaping network determined, it is necessary to design the circuit that synthesizes the required function. The discussion of Section 11.5.3 mentioned the use of superdiode connections to improve the sharpness of break points compared to that which can be achieved with diodes alone. This technique was not used for the sine shaper, since the rounding associated with the normal diode forward characteristics actually improves the quality of the fit to the sine curve.

The compressive type nonlinearities described in Section 11.5.3 were realized using diodes to increase the feedback around an operational amplifier, thus reducing its incremental closed-loop gain when a break-point level was exceeded. An alternative is to use diodes to decrease the drive signal applied to the amplifier to lower incremental gain. This approach simplifies temperature compensation. The topology used is shown in Fig. 12.34.

The input-signal level of 20 volts peak-to-peak corresponds to the input variable range of ±90° shown in Fig. 12.33. Thus the break-point locations of ±20°, ±40°, ±60°, and ±80° correspond to input-voltage levels of ±2.22 volts, ±4.44 volts, ±6.67 volts, and ±8.89 volts, respectively. Resistor values are determined as follows. It is initially assumed that the diodes are ideal, in that they have a threshold voltage of zero volts, zero resistance in the forward direction, and zero conductance in the reverse direction. Assume that the R_1-R_2 path is to provide the break points at input voltages of ±8.89 volts. Since the inverting input of the operational amplifier is at ground potential, the resistor ratio necessary to make the voltage at the midpoint of these two resistors ±1.5 volts with ±8.89 volts at the input is

$$\frac{R_2}{R_1 + R_2} = \frac{1.5}{8.89} = 0.1687 \tag{12.72}$$

The ratios of resistor pairs R_3-R_4, R_5-R_6, and R_7-R_8 are chosen in a similar way to locate the remaining break points.

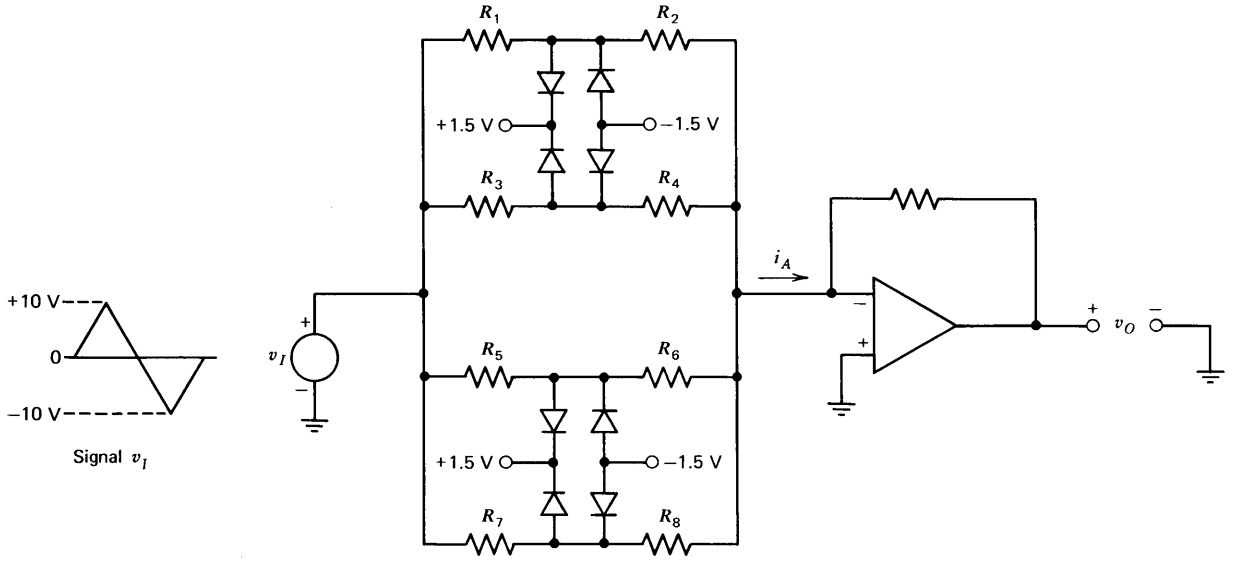


Figure 12.34 Simplified sine-wave shaper.

The relative conductances of the resistive paths between the triangular-wave signal source and the inverting input of the operational amplifier are constrained by the relative slopes of the desired transfer characteristics as follows. The closed-loop incremental gain of the connection is proportional to the incremental transfer conductance from the signal source to the current i_A defined in Fig. 12.34. With the ratio of the two resistors in each path chosen in accordance with relationships like Eqn. 12.72, the incremental transfer conductance is zero (for ideal diodes) when the input-signal magnitude exceeds 8.89 volts, increases to $1/(R_1 + R_2)$ for input-signal magnitudes between 6.67 and 8.89 volts,, increases further to $[1/(R_1 + R_2)] + [1/(R_3 + R_4)]$ for input-signal magnitudes between 4.44 and 6.67 volts, etc. If we define $1/(R_1 + R_2) = G$, realizing the correct relative slope for input-signal magnitudes between 4.44 and 6.67 volts requires

$$\frac{1}{R_1 + R_2} + \frac{1}{R_3 + R_4} = 1.879G \tag{12.73}$$

The satisfaction of Eqn. 12.73 makes the slope in this input signal range 1.879 times as large as the slope for input signals between 6.67 and 8.89 volts. Corresponding relationships couple other resistor-pair values to the R_1-R_2 pair.

The sets of equations that parallel Eqns. 12.72 and 12.73, together with the selection of any one resistor value, determine reistors R_1 through R_8. The general resistance level set by choosing the one free resistor value is selected based on loading considerations and to insure that stray capacitance does not deteriorate dynamic performance.

The circuit used for the sine shaper (Fig. 12.35) uses the standard 1% tolerance resistor values that best approximate calculated values. The five diodes labeled *A* and those labeled *B* are from two CA3039 integrated-circuit diode arrays. One member of each array modifies the bias voltages to account for the diode threshold voltages and to provide temperature compensation. The compensating diodes are operated at a current level of approximately half the maximum operating current level of the shaping diodes. While this type of compensation clearly has no effect on the conductance characteristics of the shaping diodes, the exponential diode characteristics actually improve the performance of the circuit as described earlier.

Since this circuit is intended to operate to 1 MHz (a high-speed integrated-circuit operational amplifier with a discrete-component buffer to increase output-current capacity is used), capacitors are necessary at the output of the reference-voltage amplifiers to lower their output impedance at the switching frequency of the diodes. The 1.5-V levels are derived from the

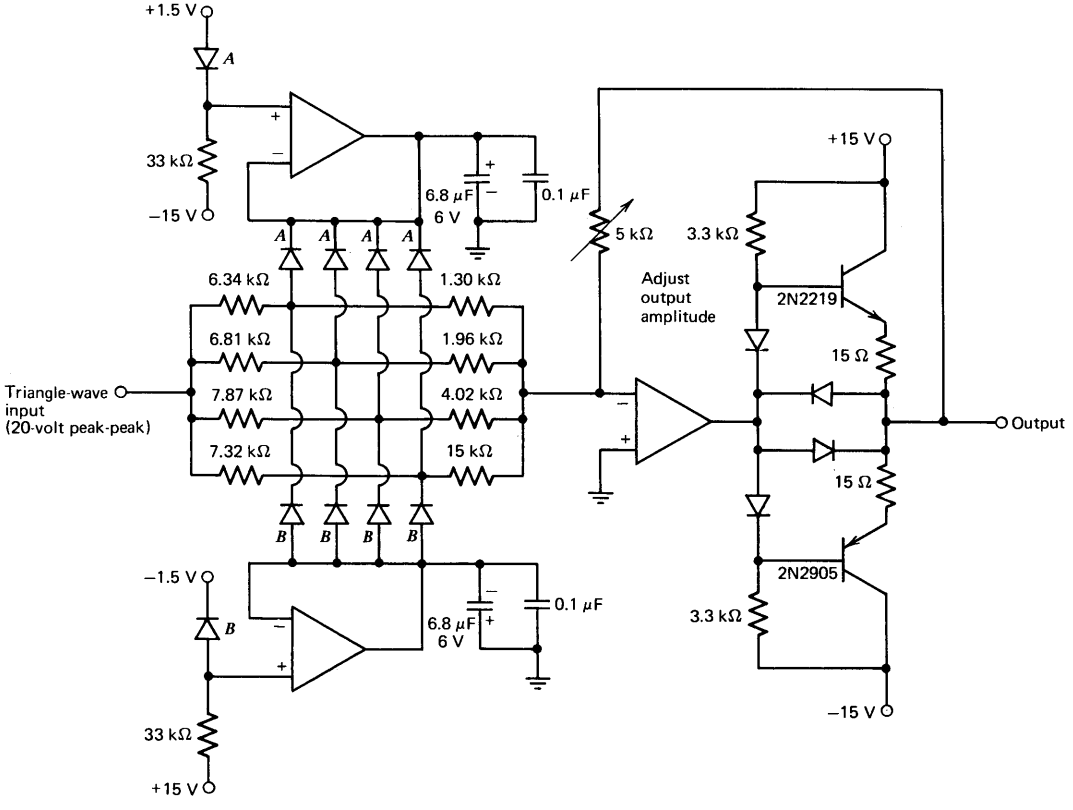


Figure 12.35 Sine-wave shaper.

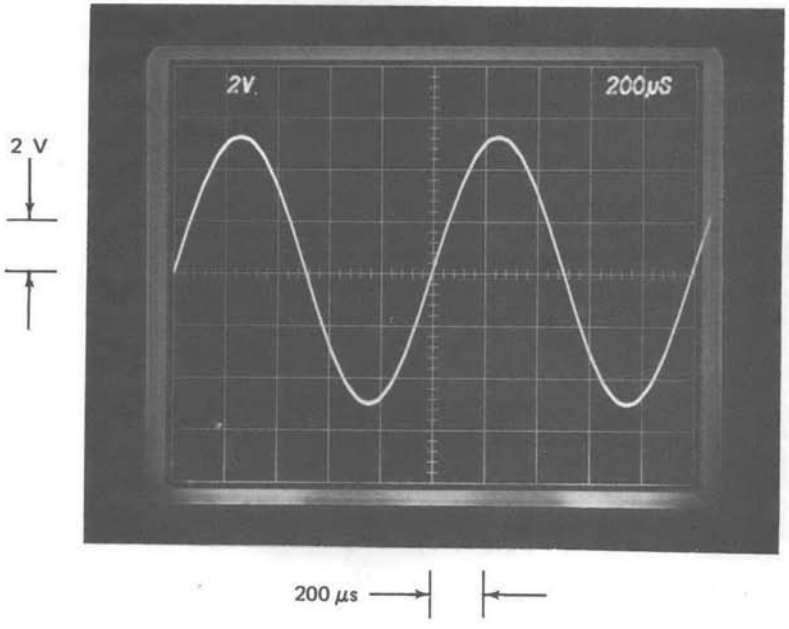


Figure 12.36 Output from sine-wave shaper.

voltages that establish triangle-wave amplitude so that any changes in this amplitude cause corresponding break-point location changes.

The circuit produces approximate sine waves with the amplitude of any individual harmonic in the output signal at least 40 dB (a voltage ratio of 100:1) below the fundamental. This performance is obtained with no trimming. If adjustments are made to null the offset of the operational amplifier, and empirical adjustments (guided by a spectrum analyzer) are used to counteract component-value errors and to compensate for finite diode forward resistance, the amplitude of individual output-signal harmonics can be reduced to 55 dB below the fundamental at low frequencies. Performance deteriorates somewhat at frequencies above approximately 10 kHz because of reduced signal-amplifier open-loop gain.

A 1-kHz output signal from the circuit is shown in Fig. 12.36.

12.5.3 A Nonlinear Three-Port Network

The realization of a device analog that may be of value in teaching the dynamic behavior of bipolar transistors requires a three-port network

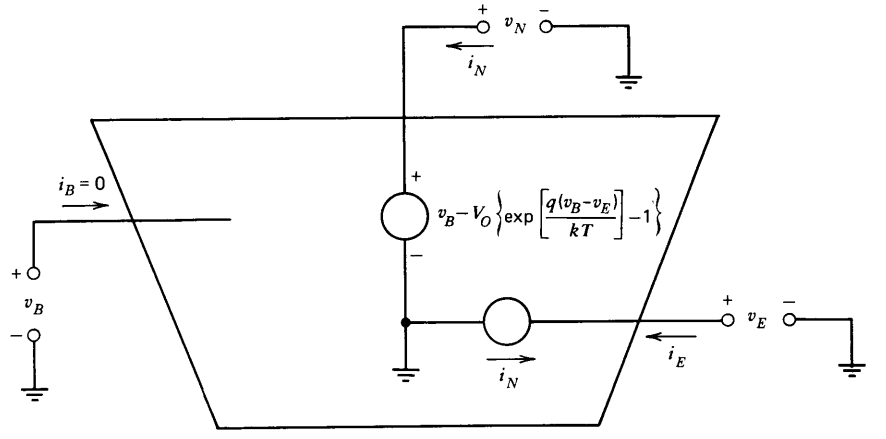


Figure 12.37 Three-port network.

defined by Fig. 12.37. The synthesis of this network is initiated by first designing a circuit that provides the relationship

$$v_N = v_B - V_O \left\{ \exp\left[\frac{q(v_B - v_E)}{kT}\right] - 1 \right\} \tag{12.74}$$

The parameter V_O, as we might expect, is related to the quantity I_S for the transistor being simulated, and consequently a corresponding temperature dependence is desirable.

There are a number of ways to simulate Eqn. 12.74. One topology that is adaptable to further requirements is shown in Fig. 12.38. Since an eventual constraint is that the current at the v_B input be zero, a buffer amplifier is used at this terminal. The second amplifier is differentially connected with an output voltage.

$$v_A = 2v_E - v_B \tag{12.75}$$

The third amplifier is also connected as a differential amplifier, so that

$$v_N = v_E - (i_T + i_A)R \tag{12.76}$$

Since feedback keeps the inverting input terminal of the third amplifier at potential v_E,

$$i_A = \frac{v_A - v_E}{R} = \frac{v_E - v_B}{R} \tag{12.77}$$

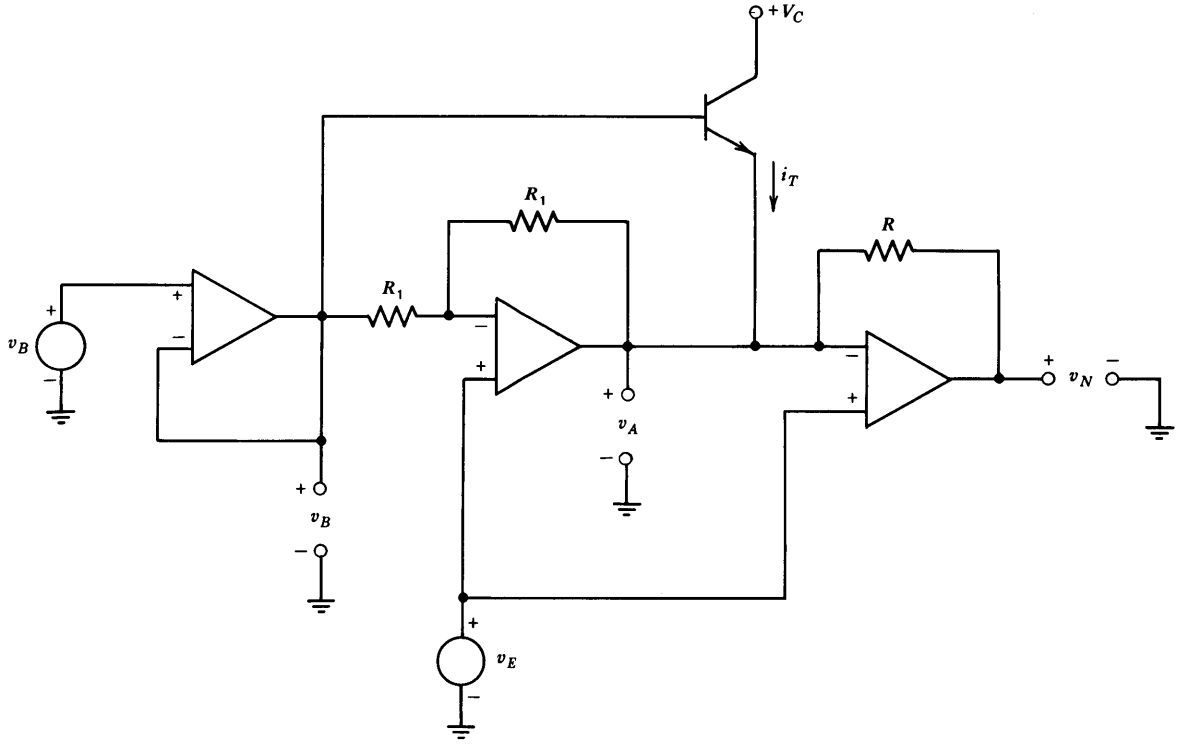


Figure 12.38 Synthesis of exponential relationship.

If we assume the usual transistor characteristics,

$$i_T \simeq I_S \left\{ \exp \left[\frac{q(v_B - v_E)}{kT} \right] - 1 \right\} \tag{12.78}$$

Substituting Eqns. 12.77 and 12.78 into Eqn. 12.76 yields the form required by Eqn. 12.75:

$$v_N = v_B - RI_S \left\{ \exp \left[\frac{q(v_B - v_E)}{kT} \right] - 1 \right\} \tag{12.79}$$

In order to complete the synthesis, it is necessary to sample the current flowing at terminal N and make the current flowing at terminal E the negative of this current. A modification of the Howland current source (see Section 11.4.3) can be used. The basic circuit with differential inputs is shown in Fig. 12.39*a*. (The reason for the seemingly strange input-voltage connection and the split resistor will become apparent momentarily.) The current i_O for these parameter values is

$$i_O = \frac{2(v_A - v_C)}{R} = \frac{2(v_A - v_A - v_I)}{R} = \frac{-2v_I}{R} \tag{12.80}$$

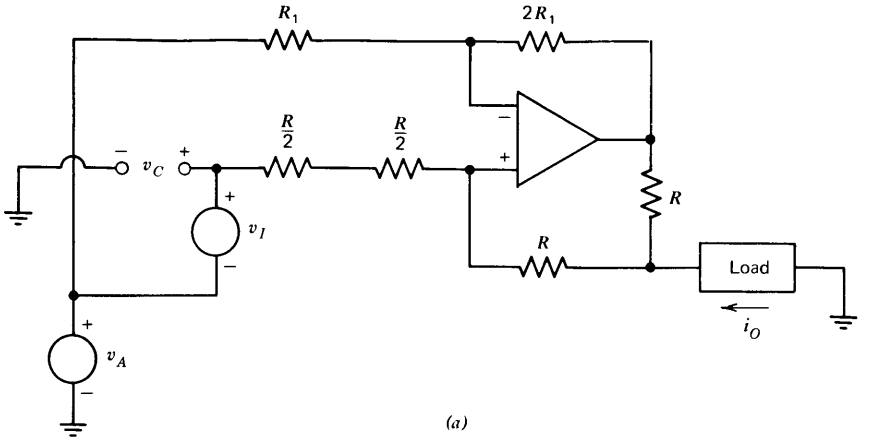
In Fig. 12.39*b*, the voltage source v_I and half of the split resistor are replaced with a Norton-equivalent circuit. For equivalence, it is necessary to make $i_I = 2v_I/R$. Expressing Eqn. 12.80 in terms of i_I shows

$$i_O = -i_I \tag{12.81}$$

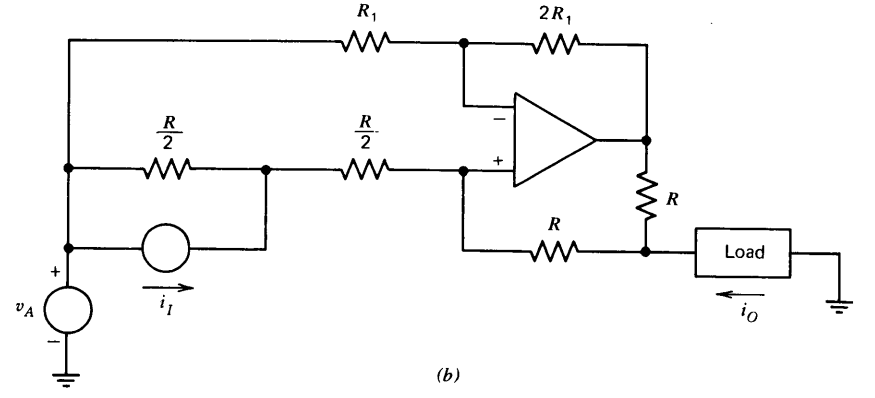
The topology of Fig. 12.39*b* shows that the i_T current source can be returned to ground rather than to voltage source v_A. This modification is shown in Fig. 12.39*c*, the current-controlled current source necessary in our present application. Note that the output is independent of v_A, the common-mode input voltage applied to the current source.

The circuits of Figs. 12.38 and 12.39*c* are combined to form the three-port network as shown in Fig. 12.40. In this circuit, the feedback for the voltage v_N is taken from the output side of the current-sampling resistor so that voltage drops in this resistor do not influence v_N. It is necessary to buffer the 100-kΩ feedback resistor with a unity-gain follower to insure that current through this resistor does not flow through the current-sampling resistor and thus alter i_E.

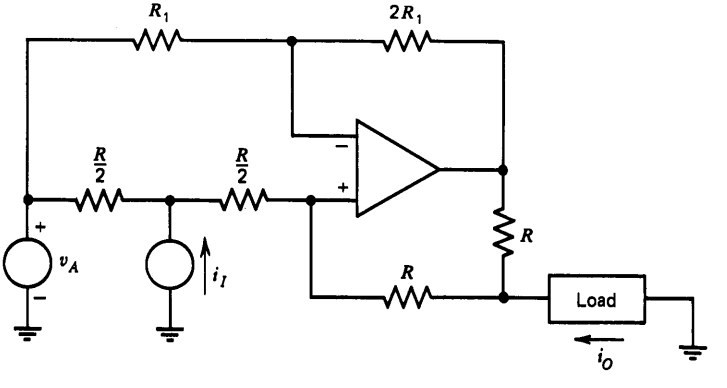
The trim potentiometer allows precise matching of resistor ratios to make current i_E independent of common-mode voltage levels at various points in the current source and thus dependent only on i_N. In this application, it was not necessary to have exactly unity gain between i_N and $-i_E$, so no trim is included for this ratio. The general magnitude of the resistors



(a)



(b)



(c)

Figure 12.39 Current-controlled current source. (*a*) Basic Howland current source. (*b*) Current source following Norton substitution. (*c*) Final configuration.

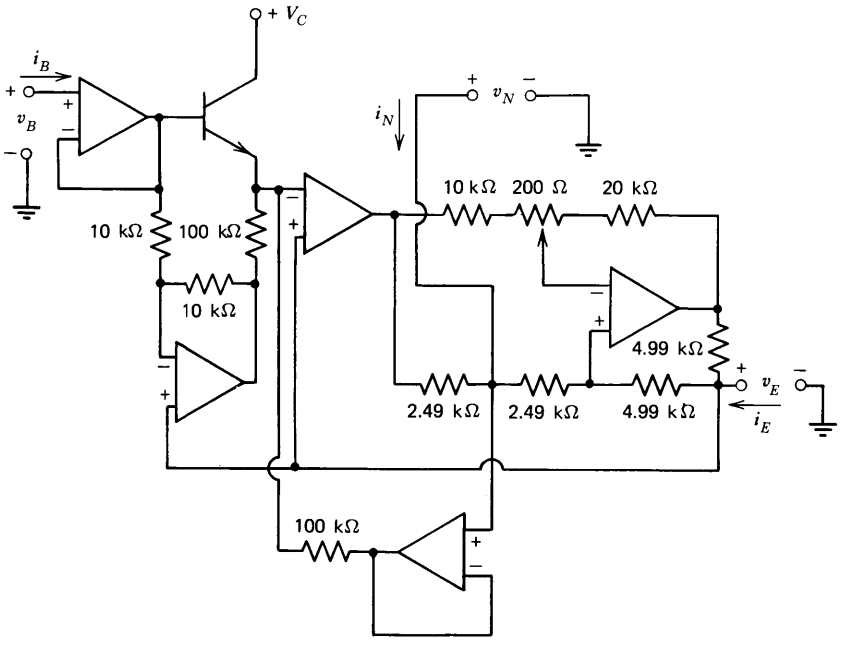


Figure 12.40 Complete nonlinear three-port network.

in the current source is chosen for compatibility with required current levels and amplifier characteristics and is not important for purposes of this discussion.

PROBLEMS

P12.1

Consider a Wien-Bridge oscillator as shown in Fig. 12.1. Show that if the output signal is of the general form $v_O = E \sin [(t/RC) + \theta]$ where θ is a constant, the signals applied to the two inputs of the operational amplifier are virtually identical, a necessary condition for satisfactory performance. Note that if the inverting and noninverting inputs are interchanged and it is assumed that the output has the form indicated above, the signals at the two inputs will also be identical. However, this modified topology will not function as an oscillator. Explain.

P12.2

A Wien-Bridge oscillator is constructed using the basic topology shown in Fig. 12.1. Because of component tolerances, the time constants of the series and parallel arms of the frequency-dependent feedback network

differ by 5%. How must component values in the frequency-independent feedback path be related to guarantee oscillation?

P12.3

Use a describing-function approach to analyze the circuit shown in Fig. 12.3, assuming that the operational amplifier is ideal and that the diodes have zero conductance until a forward voltage of 0.6 volt is reached and zero resistance in the forward-conducting state. In particular, determine the magnitude of the signal applied to the noninverting input of the amplifier and the third-harmonic distortion present at the amplifier output.

P12.4

A sinusoidal oscillator is constructed by connecting the output of a double integrator (see Fig. 11.12) to its input. Show that amplitude can be controlled by varying the magnitude of the $(R/2)$-valued resistor shown in this figure. Design a complete circuit that can produce a 20-V peak-to-peak output signal at 1 kHz. Use a FET with parameters given in Section 12.1.4 for the control element. Analyze your amplitude-control loop to show that it has acceptable stability and a crossover frequency compatible with the 1-kHz frequency of oscillation. If you have confidence in your design, build it. The 2N4416 field-effect transistor is reasonably well characterized by the parameters referred to above.

P12.5

The discussions of Sections 12.2.2 and 12.2.3 suggest operating electronic switches connected to symmetrical, variable voltages from the output of a

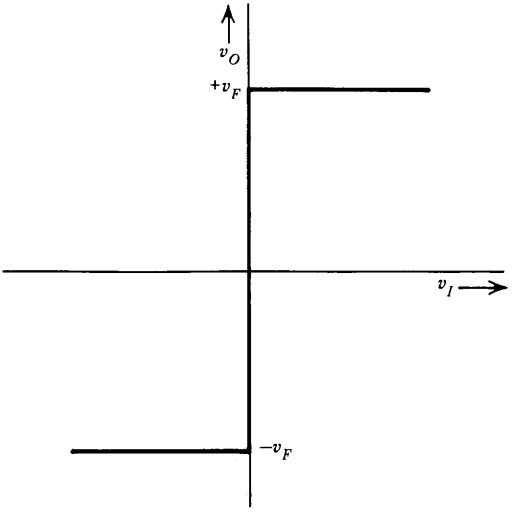


Figure 12.41 Infinite-gain limiter.

Schmitt trigger for two different applications. An alternative to the use of switches is to use a circuit that has the transfer characteristic shown in Fig. 12.41 for the necessary shaping function. (In this diagram, the voltage v_F is a positive variable.) Design a circuit that uses operational amplifiers to synthesize this transfer characteristic. Your output levels should be insensitive to temperature variations.

P12.6

A magnetic-suspension system was described in Section 6.2.3. Develop an electronic analog simulation of this system that permits determination of the transients that result from disturbing forces applied to the ball. Assume that, in addition to operational amplifiers and appropriate passive components, multipliers with a scale factor $v_O = v_X v_Y / 10$ volts are available. A way to perform the division required in this simulation using a multiplier and an operational amplifier is outlined in Section 6.2.2.

You may leave the various element values in the simulation defined in terms of system parameters, without developing final amplitude-scaled values.

P12.7

A circuit intended for use as a precision voltage reference for an analog-to-digital converter is shown in Fig. 12.42. The circuit uses a fraction of the Zener-diode voltage as its output. While this method involving resistive attenuation results in relatively high output resistance compared with using the voltage at the output of the amplifier as the reference, the output voltage becomes essentially independent of operational-amplifier offset voltage.

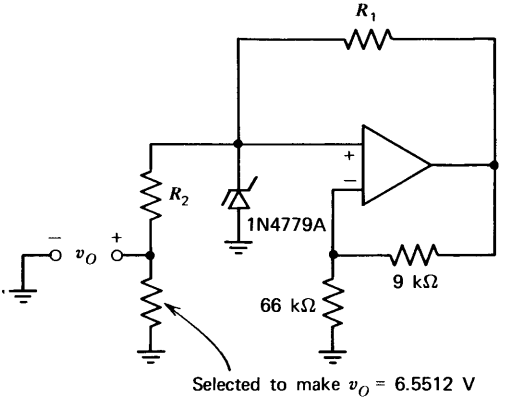


Figure 12.42 Voltage reference.

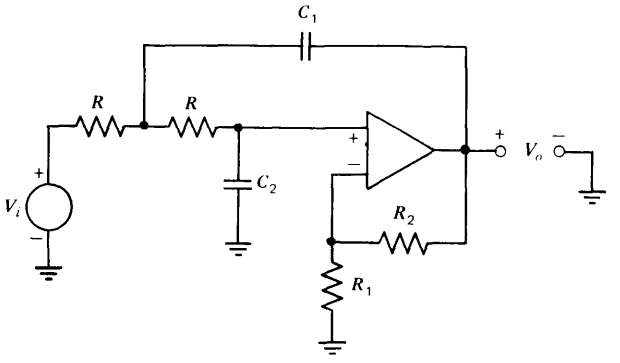


Figure 12.43 Low-pass Sallen and Key circuit with voltage gain.

The specified breakdown voltage of the 1N4779A is 8.5 volts ±5%. The indicated resistor is selected during testing to obtain the required output voltage independent of the actual value of the Zener-diode voltage.

The breakdown voltage range and the temperature coefficient of the device are guaranteed at an operating current of 0.500 mA. By proper choice of R_1 and R_2, it is possible to make the current through the Zener diode independent of the actual Zener voltage after the single indicated selection has been completed. Such a choice is advantageous since it simplifies circuit calibration as opposed to methods that require two or more interdependent adjustments to set output voltage and Zener-diode operating current. Find values for R_1 and R_2 that result in this simplification. (Please excuse the somewhat unwieldy numbers involved in this problem, but it is drawn directly from an existing application.)

P12.8

A Sallen and Key low-pass circuit with an amplifier closed-loop voltage gain greater than unity is shown in Fig. 12.43. Determine the transfer function $V_o(s)/V_i(s)$ for this circuit. Compare the sensitivity of this circuit to component variations with that of the unity-gain version.

P12.9

One way to analyze the Sallen and Key circuit shown in Fig. 12.43 is to recognize the configuration as a *positive-feedback* circuit. If the loop is broken at the noninverting input to the operational amplifier, analysis techniques based on loop-transmission properties can be used.

(a) Indicate the loop-transmission singularity pattern that results when the loop is broken at the point mentioned above. It is not necessary to determine singularity locations exactly in terms of element values.

(b) Show how the closed-loop poles of the system move as a function of the closed-loop gain of the operational amplifier by using root-locus methods that have been appropriately modified for positive feedback systems.

P12.10

Design a sixth-order Butterworth filter with a 1 kHz corner frequency by cascading three unity-gain Sallen and Key circuits.

P12.11

The fifth-order Padé approximate to a one-second time delay is

$$P_5(s) = \frac{1 - 0.5s + 0.111s^2 - 1.39 \times 10^{-2}s^3 + 9.92 \times 10^{-4}s^4 - 3.31 \times 10^{-5}s^5}{1 + 0.5s + 0.111s^2 - 1.39 \times 10^{-2}s^3 + 9.92 \times 10^{-4}s^4 + 3.31 \times 10^{-5}s^5}$$

Design an active filter that synthesizes this transfer function.

P12.12

Develop a linearized block-diagram for the system shown in Fig. 12.32, assuming that the FET is characterized by the parameters given in Section 12.1.4. Show that the loop crossover frequency is low compared to 400 Hz for any input-voltage level up to 20 volts peak-to-peak. Estimate the time required for the system to restore equilibrium following an incremental perturbation (initiated, for example, by a change in input frequency) when the input-signal amplitude is 100 mV peak-to-peak. Note that the system is not significantly disturbed by a change in input amplitude when operating under equilibrium conditions, and that therefore this relatively long settling time does not deteriorate performance.

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